# 3-D Packaging:
# A Technology Review

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June 23, 2005

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## Introduction

Traditional electronics are assembled as a planar arrangement of components on a printed circuit board (PCB) or other type of substrate. These planar assemblies may then be 'plugged' into a motherboard or card cage creating a 'volume' of electronics. This architecture is common in many military and space electronic systems as well as large computer and telecommunications systems and industrial electronics. The individual PCB assemblies can be replaced if defective or for system upgrade. Some applications are constrained by the volume or the shape of the system and are not compatible with the motherboard or card cage architecture. Examples include missiles, camcorders, and digital cameras. In these systems, planar rigid-flex substrates are folded to create complex 3-D shapes. The flex circuit serves the role of motherboard, providing interconnection between the rigid boards. An example of a planar rigid – flex assembly prior to folding is shown in Figure 1. In both architectures, the interconnection is effectively 2-D.

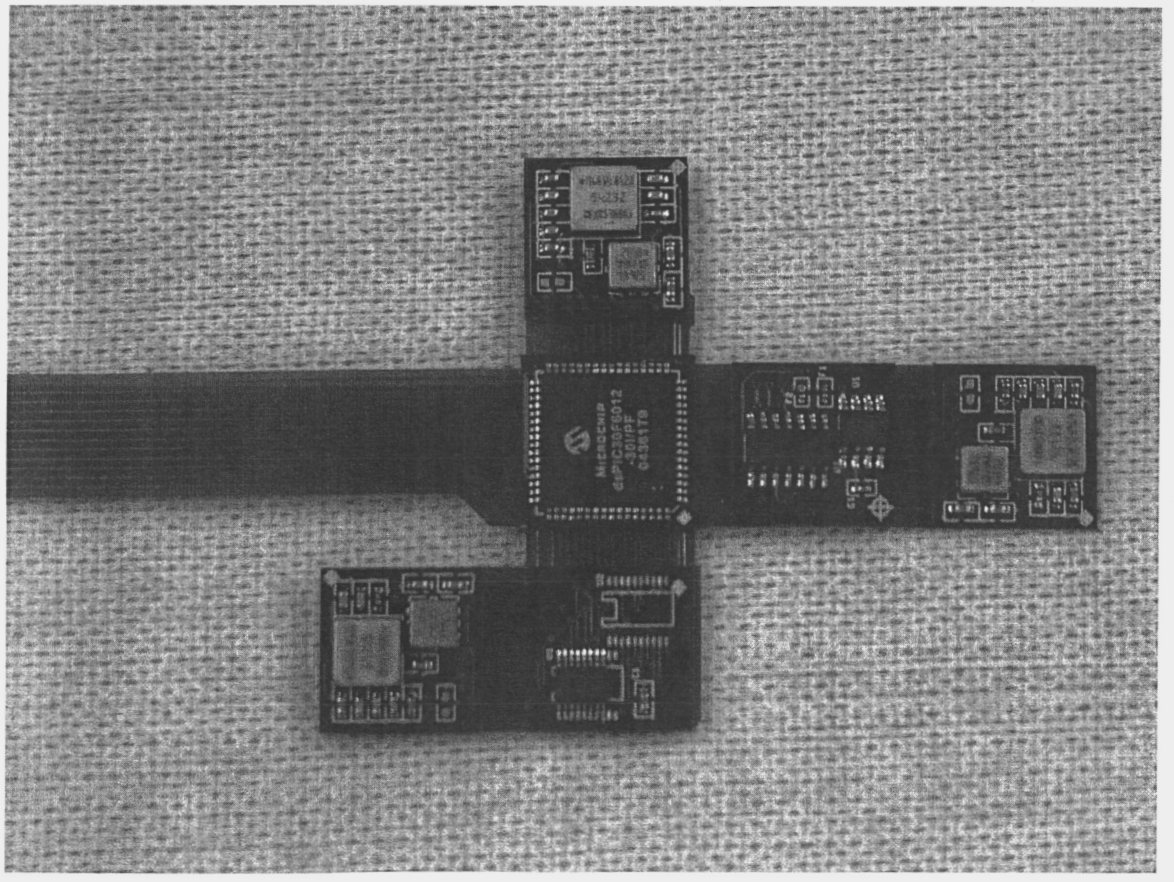


Figure 1. Example of Rigid-Flex Assembly prior to Folding. The final assembly will be folded to create a cube.

One of the earliest examples of 3-D electronics was stacked dual-in-line packages (DIPs) containing memory. Memory has a high degree of parallelism in the interconnections between devices. DIPs were stacked on top of each other. With the leads overlapping, the leads were joined by soldering, creating parallel connections to all devices in the stack. The 'chip select' pin on each package had to be individual connected – this could be accomplished with jumper wires. This is an example of Package Stacking.

Irvine Sensors pioneered Die Stacking, creating cubes of memory for solid-state data recorders. Memory die were stacked using an adhesive to form a cube. The edges of the cube were then polished to expose the edges of the wire bond pads or pad extensions. The edges of the cube were metallized and pattered, electrically interconnecting the memory die. An example of a memory cube is shown in Figure 2.

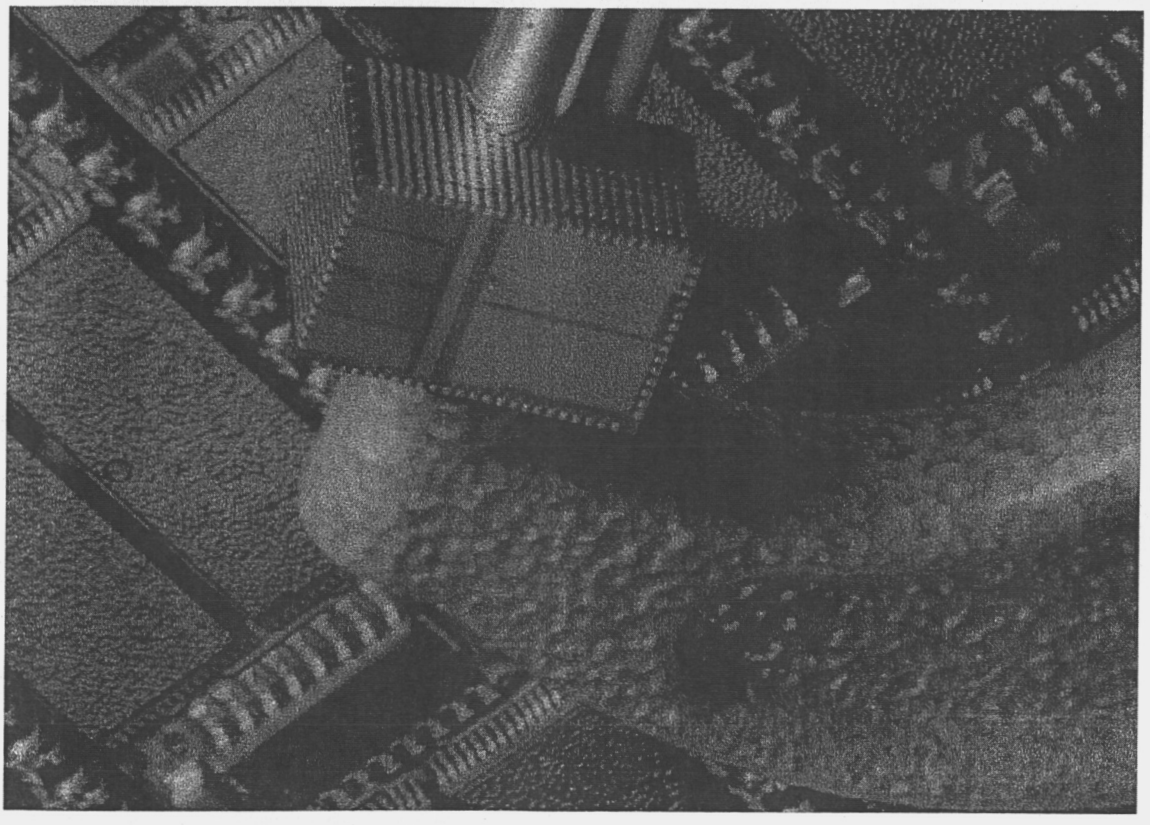


Figure 2. Example of Irvine Sensors Memory Cube.

With the rapid growth in portable consumer electronics, most notably the cell phone, the need to decrease size and weight while increasing functionality has been driving the electronics industry to widespread use of die and package stacking. Figure 3 plots the projected growth of cell phones and stacked chip scale packages (S-CSPs) [Amand.pdf]. Many approaches have recently been developed for die and package stacking.

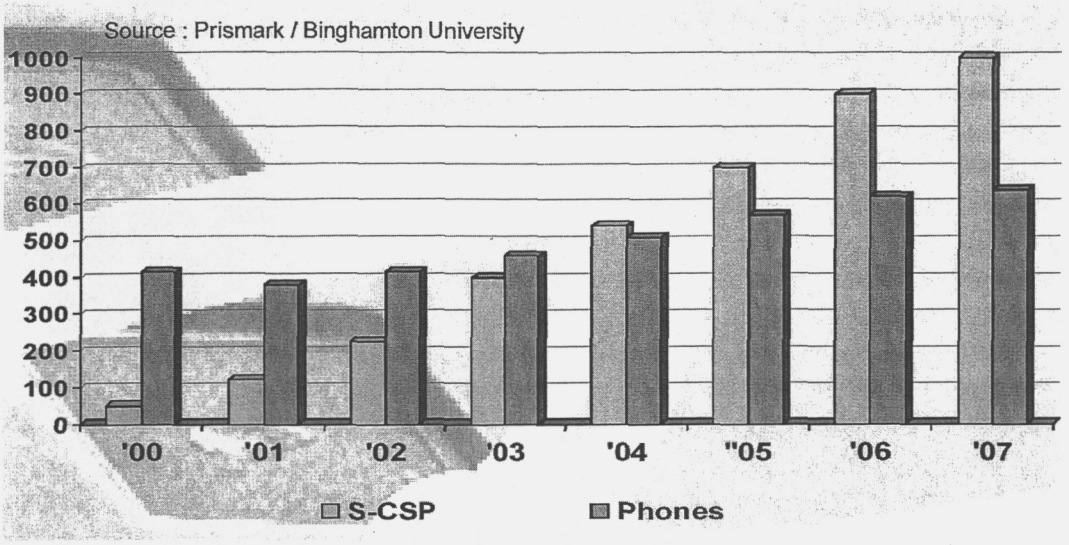



Figure 3. Projected Market for Cell Phones and Stack Chip Scale Packages. [Amand.pdf]

At the next higher level of integration, 2-D modules are being stacked to create 3-D module assemblies. One example of this is the Vertical InteGration for Opto and Radio (VIGOR) subsystems illustrated in Figure 4. This was a European Union funded 3-D Integration project [Alexandre.pdf]. The concept is similar to the Irvine Sensors die stacking approach. Individual circuit boards are assembled, tested, stacked, molded, and the edges of the cube are metallized and patterned to form the z-axis interconnections.

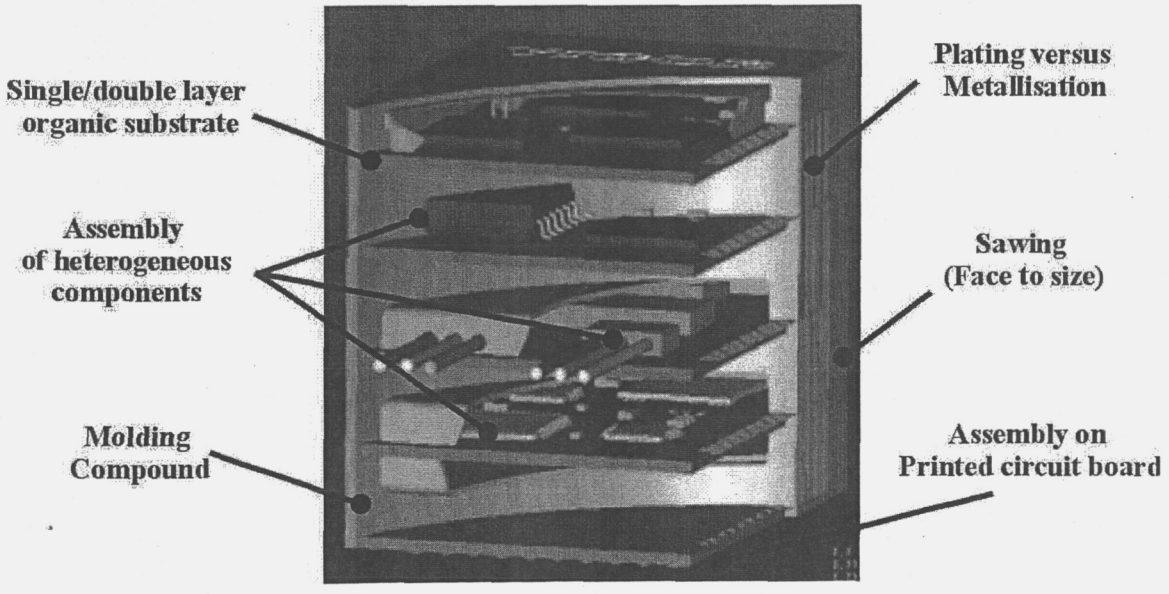



Figure 4. Illustration of 3-D Module Stacking. [Alexandre.pdf]

The ultimate in 3-D integration is wafer stacking. The technology is being developed for image processing systems. Image sensors are 2-D arrays of sensors or pixels. In current architectures, the information from each pixel must be clocked to the edge of the array

before processing. For large arrays, this serial processing does not permit real-time imaging. In wafer stacking, the processing elements are fabricated on wafers to be bonded below the sensor array. Each pixel has a processor associated with it, resulting in a massively parallel system. A top view of a two wafer stack and the cross-section of a three wafer stack are shown in Figures 5 [Guarini.pdf] and 6 [Keast.pdf], respectively.

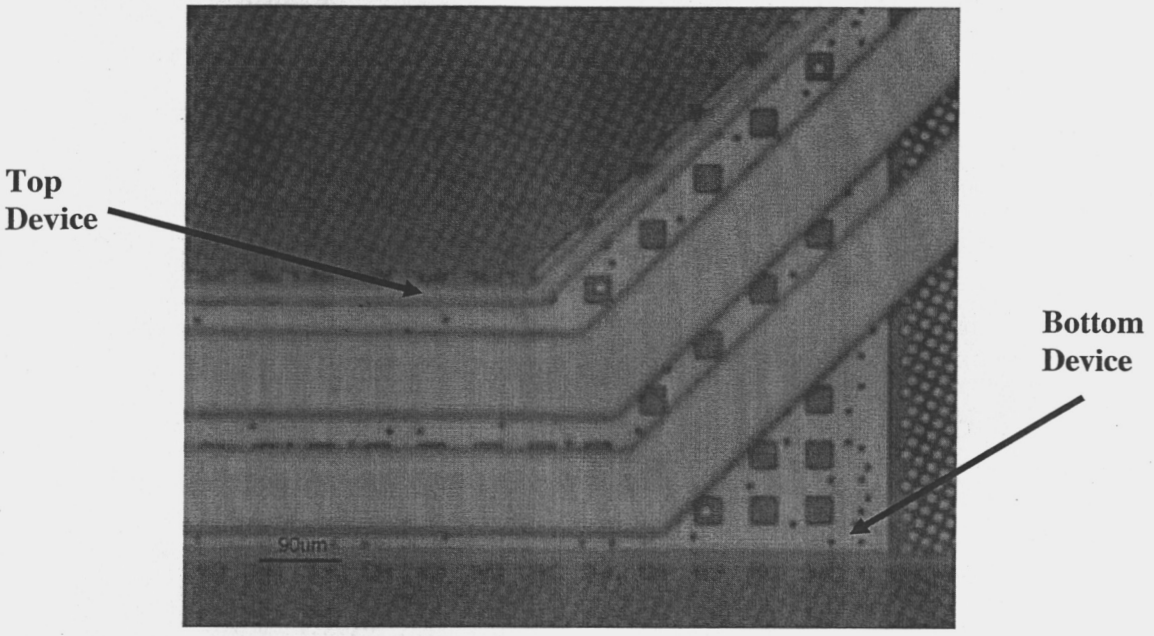



Figure 5. Image of a Two Wafer Stack. [Guarini.pdf]

The primary driver for 3-D electronics has been to reduce size and weight. Recently, 3-D electronics are being developed to reduce signal propagation delay by locating devices closer together.

The challenges faced by 3-D integration are: limits in interconnectivity in the z-axis, yield, and thermal management. Many of the 3-D approaches provide z-axis interconnection along the perimeter of the assembly and not a true 3-D interconnection distributed within the volume of the assembly. This perimeter routing limits the ability to route interconnections and also increases the signal path (all signals have to come to the edge). Pre-test and high assembly processing yields are critical to achieving a high final yield. In most 3-D constructions, rework is difficult or impossible. Finally, heat transfer to the surrounding environment by convection and conduction is limited by the available surface area. 3-D electronics have the potential to dramatically increase the heat density while simultaneously dramatically reducing the surface area of the assembly. Thus, not all electronics will be conducive to 3-D integration without significant investment in thermal management technologies.

In the following sections, the different 3-D technologies will be examined in terms of construction, applications, reliability and maturity. The limitations of each will also be discussed.

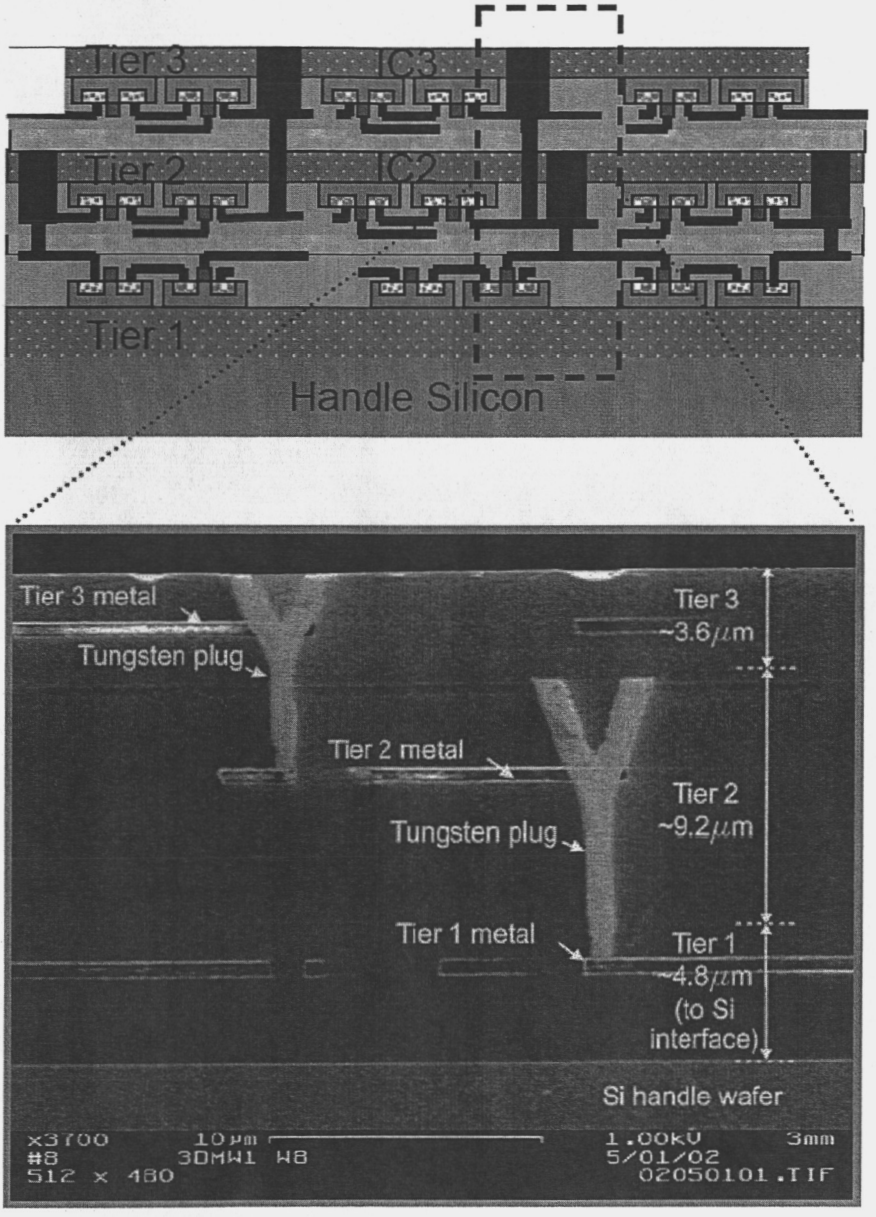
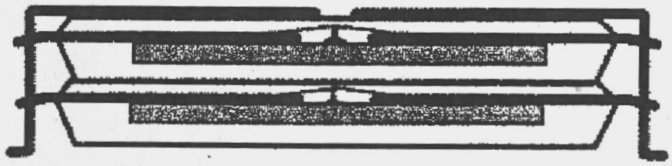


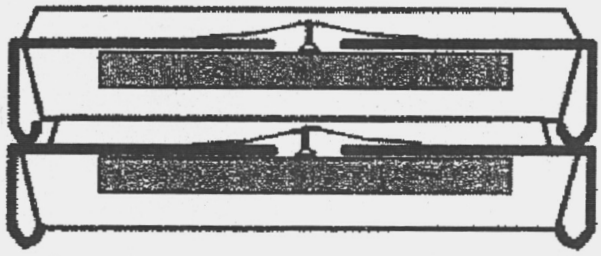

Figure 6. Cross Section of a Three Wafer Stack. [Keast.pdf]

**Package Stacking**

Package stacking is the simplest to implement. It does require internal and/or external package modification. Parallel I/O connections such as Address and Data as well as Power and Ground can share common leads for all devices. However, Chip Select for each package must be on a different pin. Figure 7 illustrates the stacking of TSOPs and SOJ packages [Cho.pdf].



**(a) 2-high TSOP stack**



**(b) 2-high SOJ stack**

Figure 7. Illustration of Stacked Lead Frame Packages. [Cho.pdf]

Figures 8 and 9 illustrate stacking of memory TSOPs to create a 32 bit wide data bus using two 16 bit devices [Priore.pdf]. In this case a perimeter substrate is used to interconnect the two TSOPs and provide Chip Select and other electrical signal routing. The solder balls shown as 67 through 87 in Figure 9 provide the electrical contacts for the extra routing required.

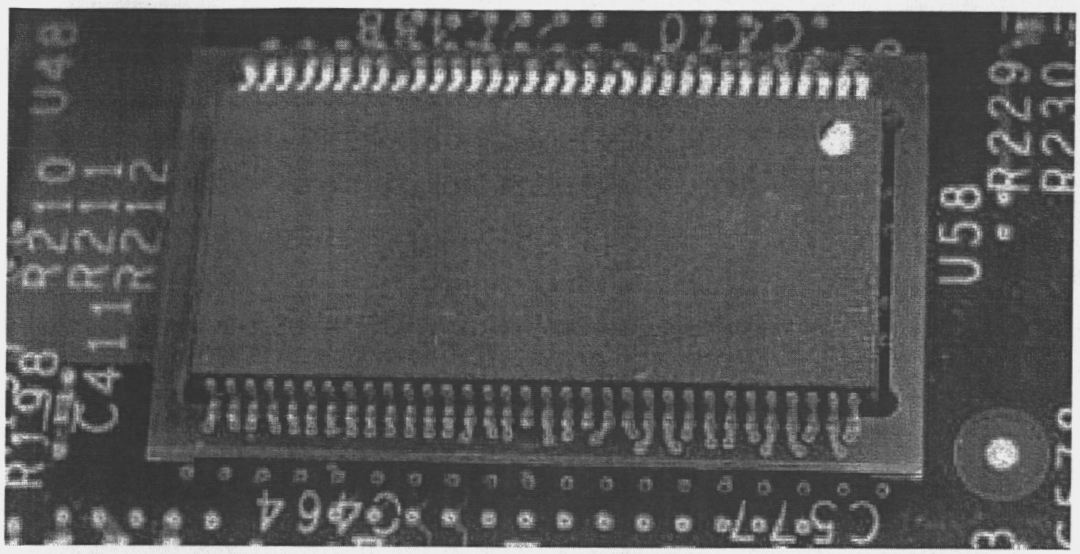



Figure 8. Photograph of a TSOP Stack. [Priore.pdf]

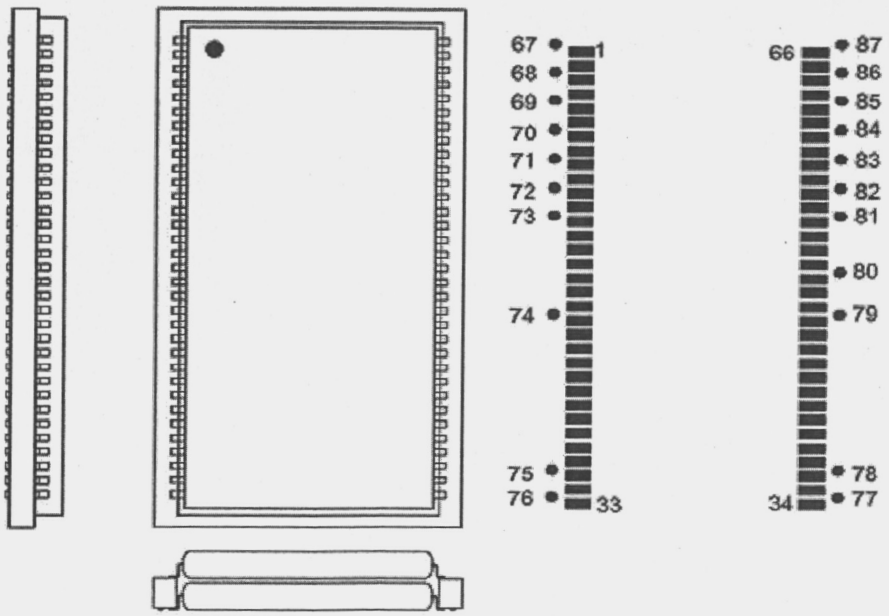



Figure 9. Illustration of the TSOP Stack. [Priore.pdf].

With the wide-spread usage of ball grid array (BGA) and chip scale packages (CSPs), stacking of these packages has become common in the portable electronics industry Figures 10 - 12 show a stacked rigid substrate CSP [etCSP.pdf].. Figure 13 shows a 4 package stack with flex substrate CSPs [Solberg-1.pdf]. The stacked packages can also contain stacked die within one or more of the packages as shown in Figure 14 [Carson.pdf]. The inclusion of a substrate (rigid or flex) in the package provides the option for the necessary routing changes for electrical connections within the stack. The packages can be stacked by the package manufacturer and assembled as a single unit by

the PCB assembler or the packages can be stacked and assembled to the PCB simultaneously by the PCB assembler. With solder ball based packages, the upper packages can be assembled with a flux dip, placement and reflow – no solder paste is required [Demmin.pdf].

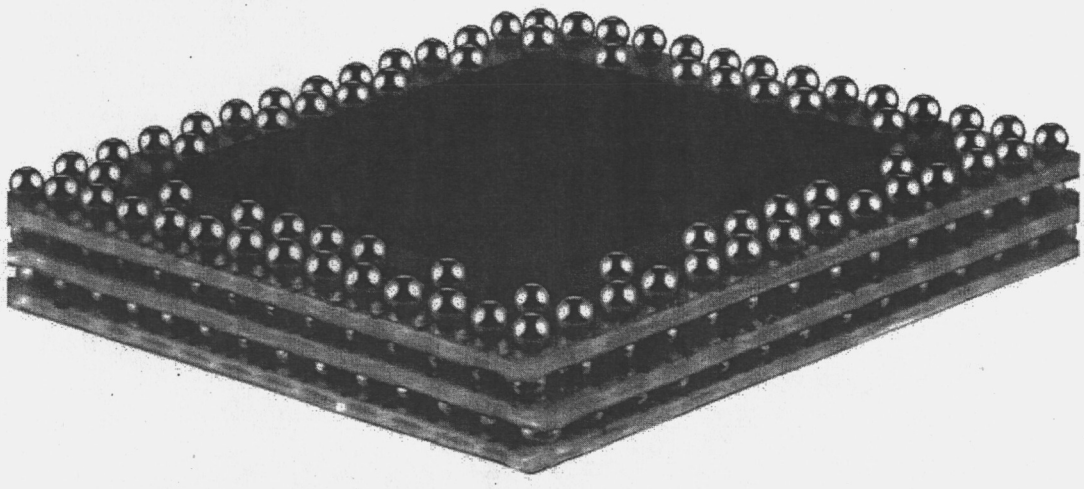


Figure 10. Stacked etCSP™ Isometric Side View. (Courtesy of Amkor)

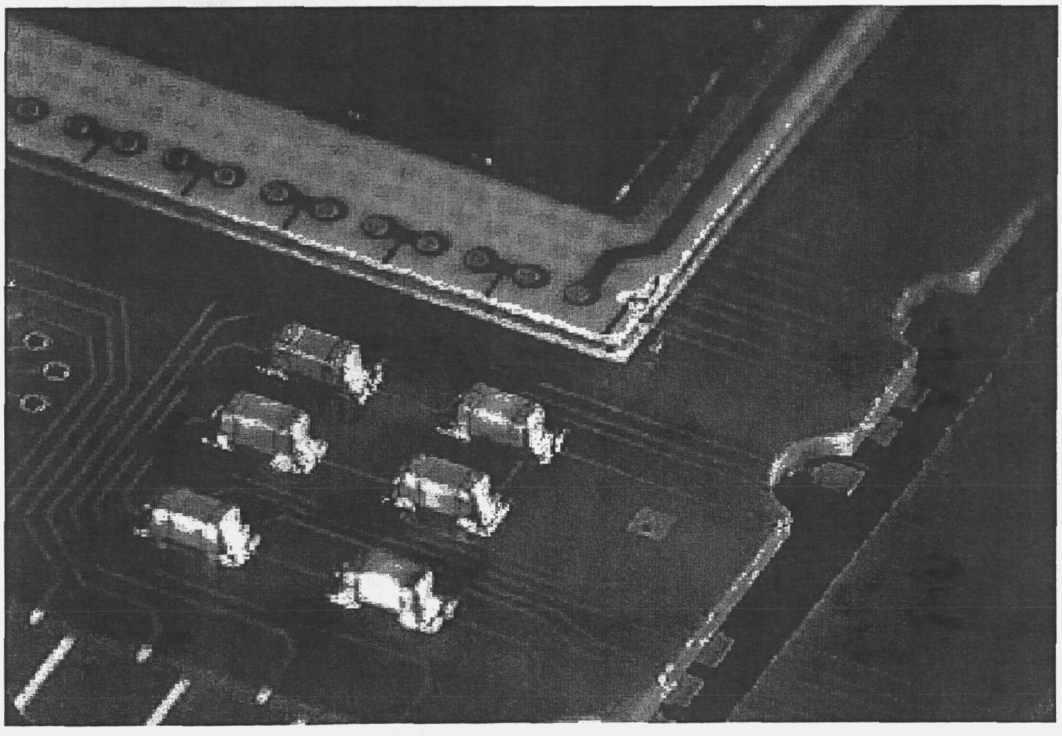


Figure 11. Photograph of a Two-Package Stack Assembled to a PCB. (Courtesy of Amkor)

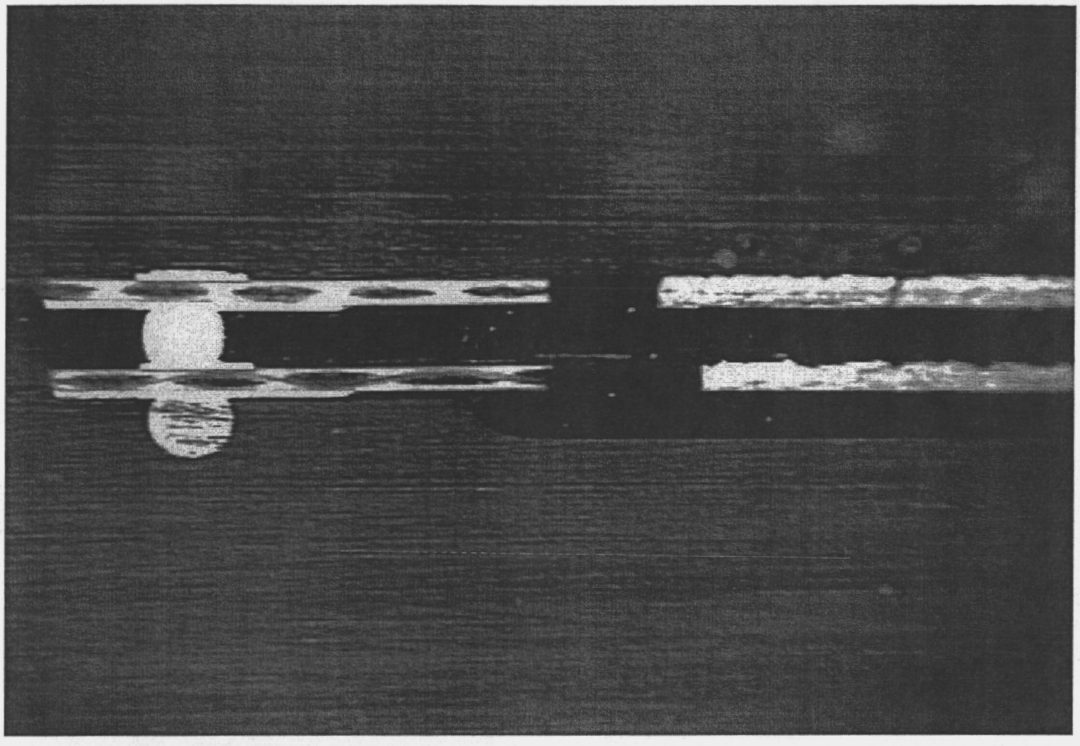


Figure 12. Cross-Section of a Two-Package Stack. (Courtesy of Amkor)

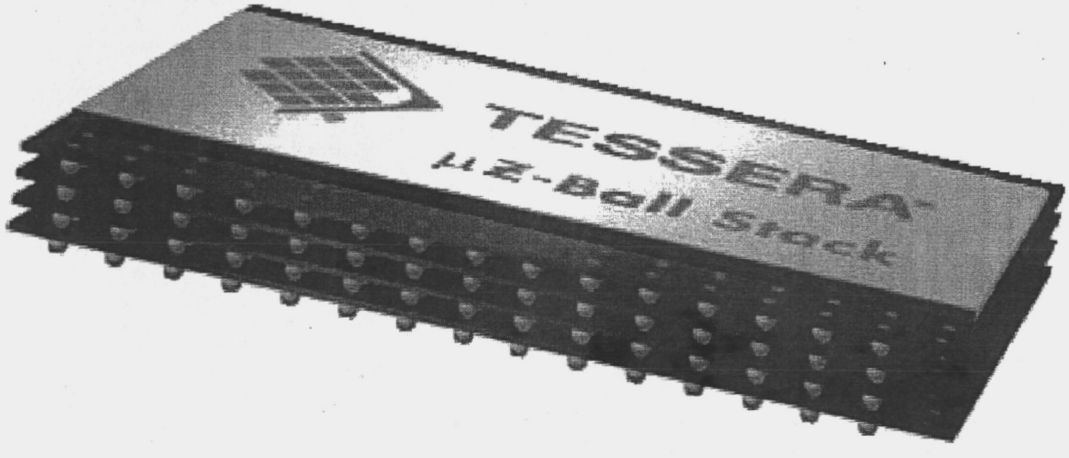



Figure 13. Example of Stacked Flex Substrate Based CSPs. [Solberg-1.pdf]

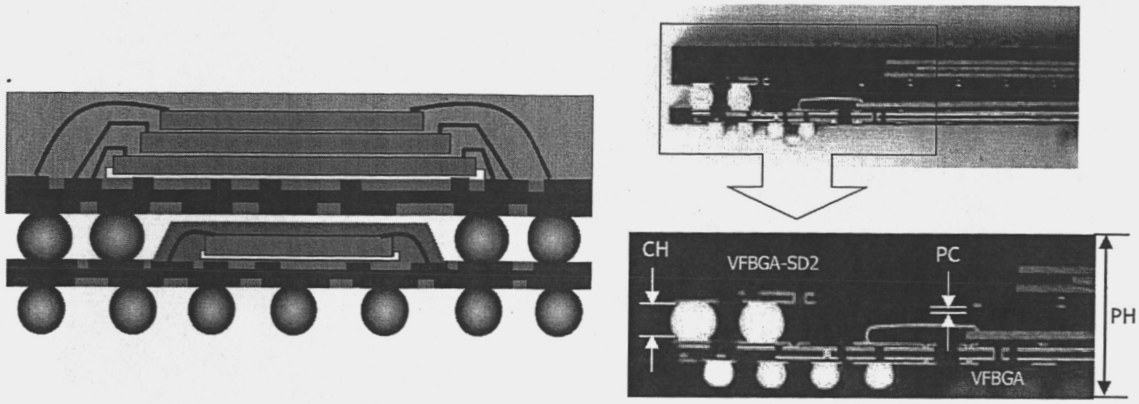



Figure 14. Stacked Packages with Stacked Die in Package. [Carson.pdf]

Irvine Sensors has developed technology to process existing packages into thin stackable layers [Gann-1.pdf]. The concept using TSOPs is illustrated in Figures 15 and 16. Similar thinning of BGAs with deposited surface metallization on the thinned layer to route from the die I/O to the layer edge has also been described by Irvine Sensors (Figure 17). Once the thinned layers are stacked and molded, the edges of the cube are metallized to connect between layers.

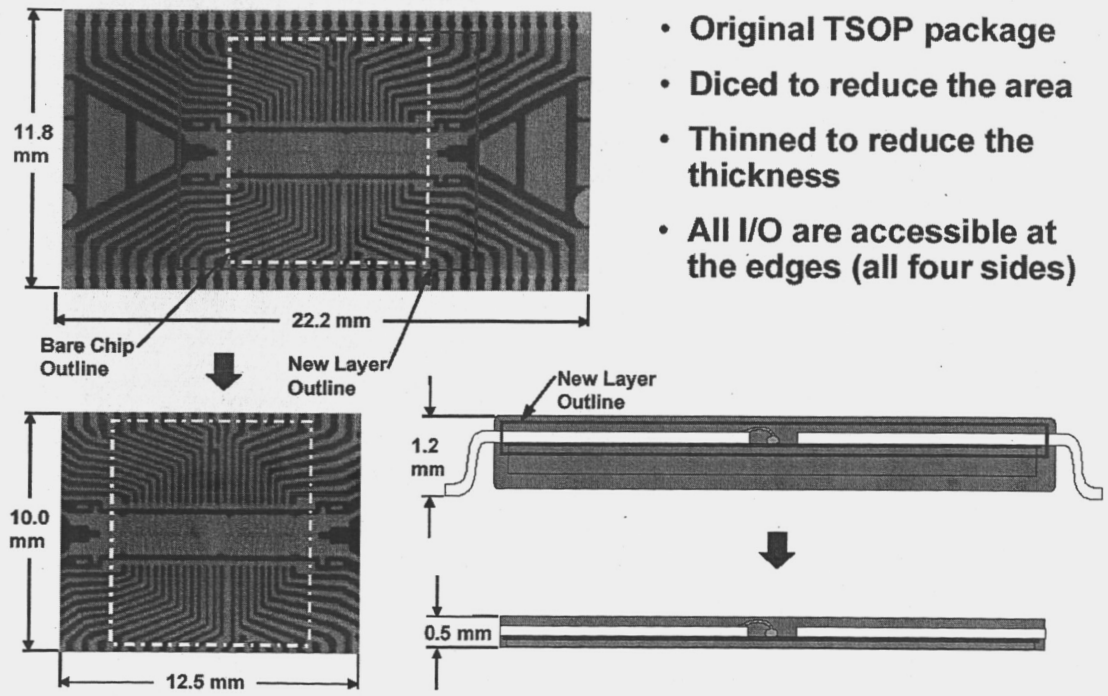



Figure 15. Irvine Sensor's Approach to Creating Thin Stackable Layers from Packaged Die. [Gann-1.pdf].

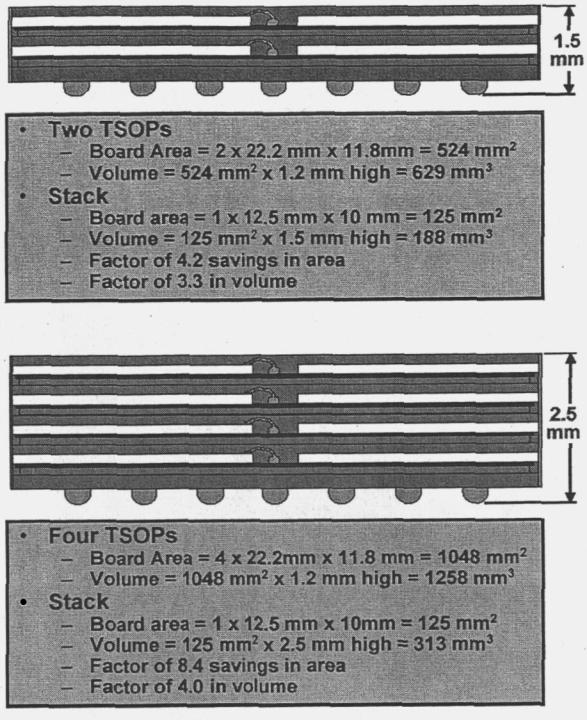



Figure 16. The Thinned Layers are Stacked and Metallized along the Edge of the Cube. [Gann-1.pdf]

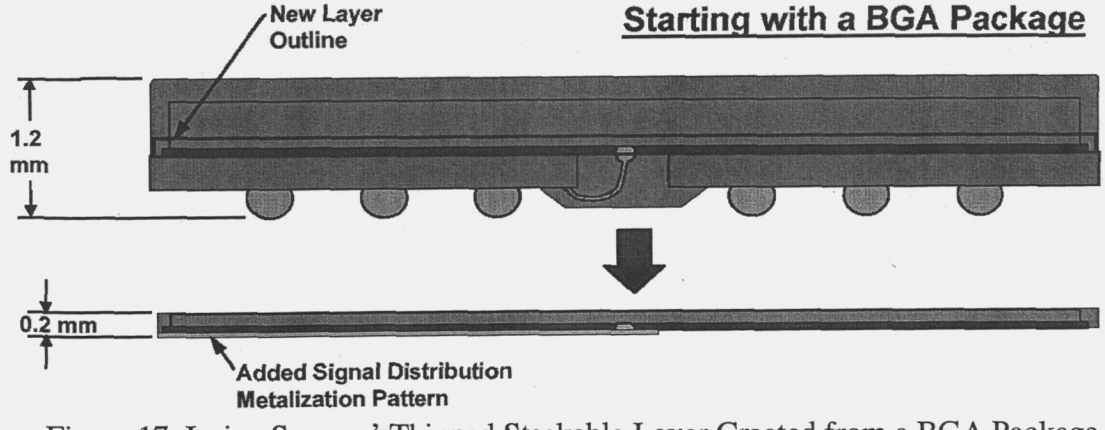



Figure 17. Irvine Sensors' Thinned Stackable Layer Created from a BGA Package. [Gann-1.pdf].

3D-Plus has also developed a 3D stacking approach for TSOP's [Val-1.pdf]. The process flow is illustrated in Figure 18. The processing is similar to the Irvine Sensors approach, but does not include package thinning. This process can be extended to other package types.

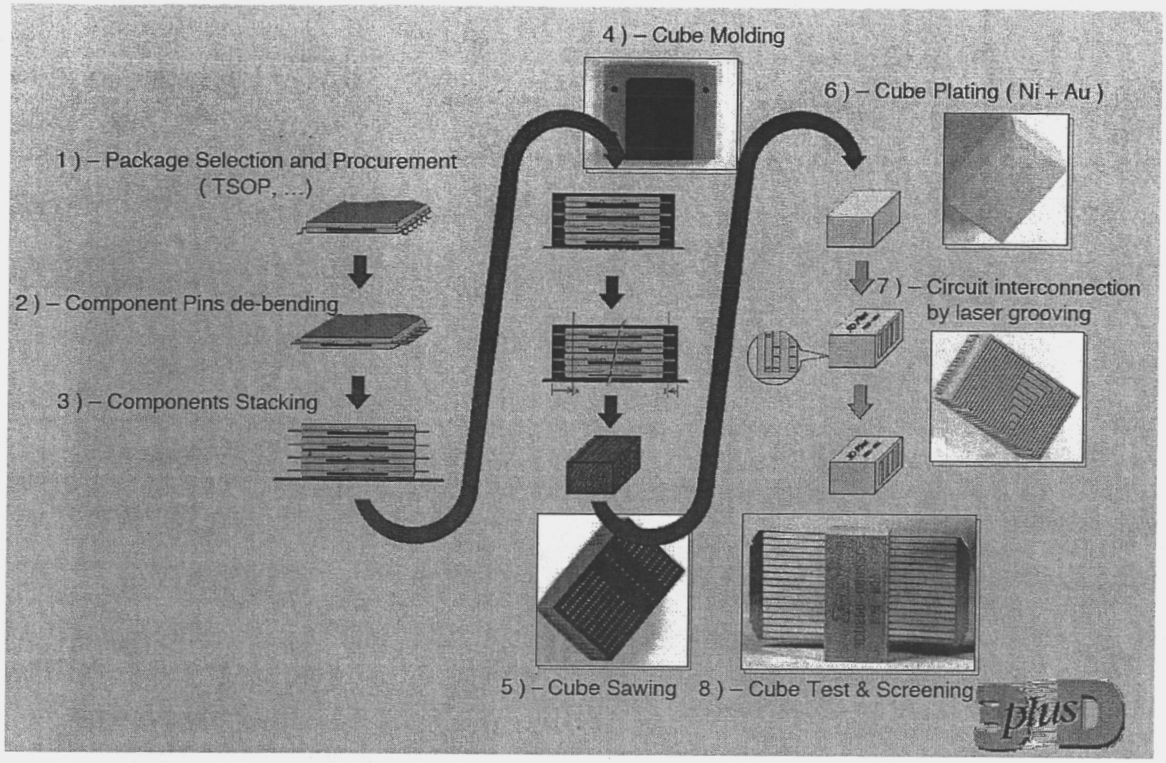



Figure 18. 3D-Plus TSOP Stacking Process. [Val-1]

Benefits of Package Stacking: The primary advantages of package stacking are the reduction in substrate area, decreased interconnection lengths and the ability to pre-test packages before stacking. Solberg has discussed the increased electrical performance with packaging stacking [Solberg-2.pdf]. The net volume and weight are not reduced by package stacking (except in the Irvine Sensors approach), but the board area occupied by the stack is less than that required to arrange the individual packages in an area configuration. The electrical interconnection length between packages in a stack is less than the length that could be achieved with individual packages arrayed in a planar configuration, decreasing propagation delay. A major advantage of this approach is the ability to pre-test and burn-in devices prior to stacking. Depending on individual die yield this can have a significant impact on the yield of the stack. Rework of a package within the stack is possible, but is much more complicated than removal of a single package configuration.

Limitations of Package Stacking: BGAs and CSPs must be designed for package stacking to allow contact pads for assembly on both the top and bottom side of the package substrate. In the case of surface mount lead frame packages, the lead length must be increased to allow lead-to-lead contact when stacked or an interposer substrate must be used. The package internal routing must also be changed to accommodate the special electrical signal routing requirements for package stacking. While BGAs and CSPs typically provide full area array I/O interconnections, packages designed for stacking are restricted to one or more rows of perimeter I/O connections. Thus, with the exception of the bottom package, the I/O count is limited or the size of the package must be increased

to allow extra rows of I/O's. Stacked packages are most appropriate for memory or memory with one high I/O count device (microprocessor, DSP, ASIC) on the bottom. Since package stacking requires the complete packaging of the individual die, there is no cost savings in the packaging process. The extra processing in the Irvine Sensors approach adds cost, but reduces height and weight.

Since heat removal through the leadframe or the solder balls to the PCB is the predominate path for conductive heat flow, stacking packages increase the thermal path length for the top package and increases the heat flux through the solder balls or leadframe of the lower packages. Also, thermal solder balls, commonly used in BGAs can only be used on the bottom package. With packages stacked, the heat transfer by natural convection from the package surface is reduced for the lower packages in the stack. Package stacking is typically restricted to low power dissipation applications and the highest power dissipating package is placed at the bottom of the stack.

Reliability: Stacked packages utilize commercial-off-the-shelf (COTS) packaging which establishes the reliability baseline. The unique reliability issues with package stacking are assembly quality and mechanical shock and vibration effects. Warpage of area array packages and the resulting impact on solder joint shapes during package stacking must be considered [Kian.pdf, Kim.pdf]. If one package warps concave and one package warps convex, the solder joints will be elongated or opens may even occur during assembly. The reliability of these elongated solder joints is a concern and must be investigated. The issue of warpage is dependent on the package style, materials and construction processes and will require investigation on an individual basis.

Increasing the mass and height of the stack assembly will potentially impact the reliability in a mechanical shock and vibration level. Currently, most package stacks are only two packages high and with the use of thin packages, the resulting height and mass is very similar to conventional non-stacked packages. Little data is available on mechanical testing of more than two packages stacked. This area will need further analysis and experimentation before stacked packages could be used in NASA applications.

The following tables provide published reliability data for different stacked packages. The testing is not to failure, so failure statistics can not be used to predict failure rates.

Table 1. Reliability for a Two Package Stacked CSP (Flex based substrate) with Sn-3.0Ag-0.5Cu Solder Balls. [Demmin.pdf]

| Test | Read Point | Result (fails) |
|---|---|---|
| Moisture Sensitivity | Level 2 | 0/11 |
| Thermal Cycling Board Level | 1000 cycles | 0/31 |
| Unbiased Autoclave | 168 hrs | 0/10 |
| High Temperature Storage | 1000 hrs | 1/11 |
| Drop Test | 30 drops, 1500g | 1/18* |
| Vibration | 20 mins/axis | 0/17 |

* package-board interconnect level solder joint failure

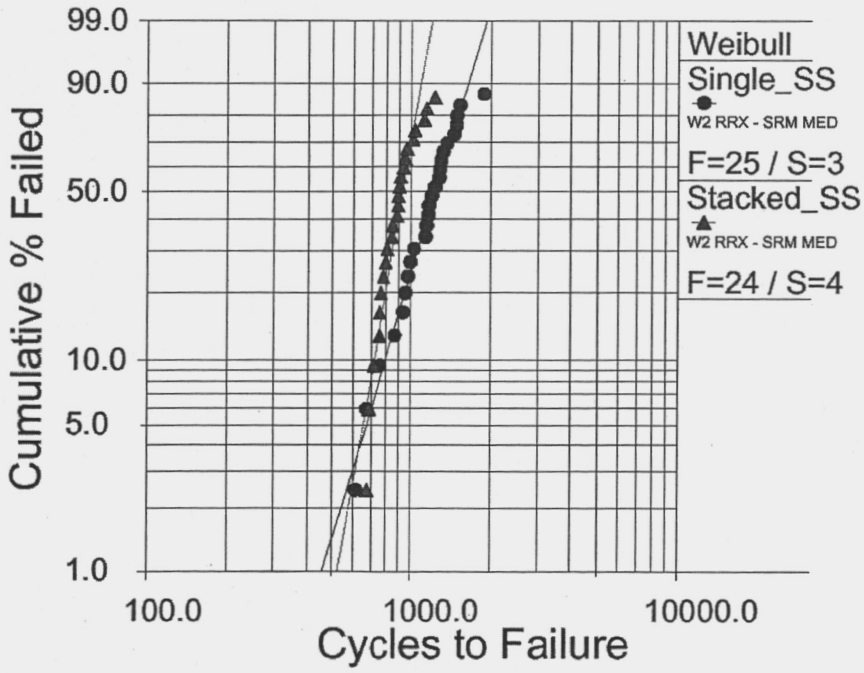
Table 2. Reliability for a Two Package Stacked CSP (Flex based substrate) with eutectic Sn-Pb Solder Balls. [Demmin.pdf]

| Test | Read Point | Result (fails) |
|---|---|---|
| Moisture Sensitivity | Level 2 | 0/22 |
| Unbiased Autoclave | 96 hrs | 0/19 |
| Drop Test | 30 drops, 1500g | 0/18 |
| Vibration | 20 mins/axis | 0/18 |

Table 3. Reliability for a Four Package Stacked CSP (Flex based substrate) with eutectic Sn-Pb Solder Balls. [Demmin.pdf]

| Test | Read Point | Result (fails) |
|---|---|---|
| Moisture Sensitivity | Level 2 | 0/11 |
| Thermal Cycling Board Level | 1000 cycles | 0/31 |
| Unbiased Autoclave | 168 hrs | 0/19 |

Amkor has studied the thermal cycle reliability (-40°C to 125°C, 1 cycle/hour) of two stacked CSPs (rigid substrate) versus a single CSP. Figure 19 is a Weibull plot of two stacked CSPs and a single CSP assembled on one side of a laminate substrate. As can be




β1=4.2934, η1=1347.6534, ρ=0.9858
β2=7.4308, η2=976.0282, ρ=0.9395

Figure 19. Weibull Plot of Thermal Cycle (-40°C to +125°C) for a Single CSP and a Two Stack CSP on a Single Side of a Laminate Substrate. [Kim.pdf]

seen, the mean life is slightly lower for the two stacked CSPs. Figure 20 compares the results (modeled and measured) mean life with single CSPs and two stacked CSPs on a single side (SS) of the laminate and on both sides (DS). In both cases, the thermal cycle reliability of the two stacked CSPs is less than that of the single CSP. Stacking CSPs leads to an increase in assembly stiffness, which reduces reliability [Kim.pdf]. Stacking additional CSPs would lead to a further increase in stiffness.

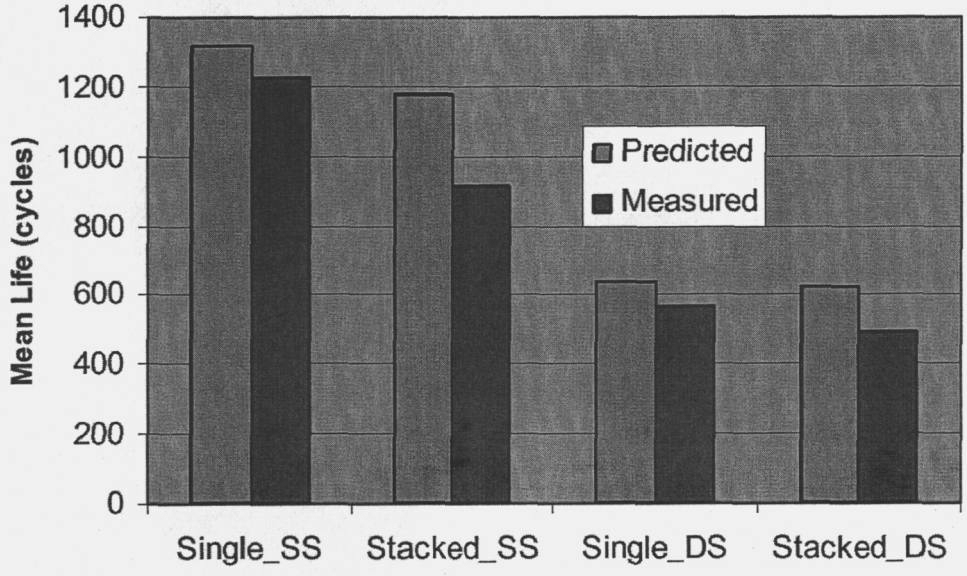



Figure 20. Experimentaly Measured and Model Predicted Mean Life of Single and Two Stack CSPs in a Single Sided (SS) or Double Sided (DS) Laminate Assembly. [Kim.pdf]

Technology Readiness Level Assessment: Stacked packages have been demonstrated in portable consumer electronics. These products have a limited life expectancy and with the exception of mechanical shock a relatively benign operating environment. A TRL of 3 is assigned to stacked package technology. This is based on the limited flight experience with non-stacked BGAs and CSPs and the lack of laboratory reliability testing of stacked packages for space environmental conditions and requirements.

**Die Stacking**

The most rapidly growing segment of the 3-D market is die stacking. The earliest implementations pioneered by Irvine Sensors involved stacking die using adhesives to create a cube, polishing the edge(s) to expose the perimeter wire bond pads or pad extensions, then passivation and metallization of the cube edges to provide z-axis interconnectivity (Figure 21). The resulting 3-D memory cubes were used for solid-state data recorders. Caterer, et.al. used a thick polyimide layer to redistribute the memory die I/O to the edge of the die for routing along the cube edge (Figures 22 and 23) [Caterer.pdf]. The cube was assembled to the package using Sn/Pb solder bumps.

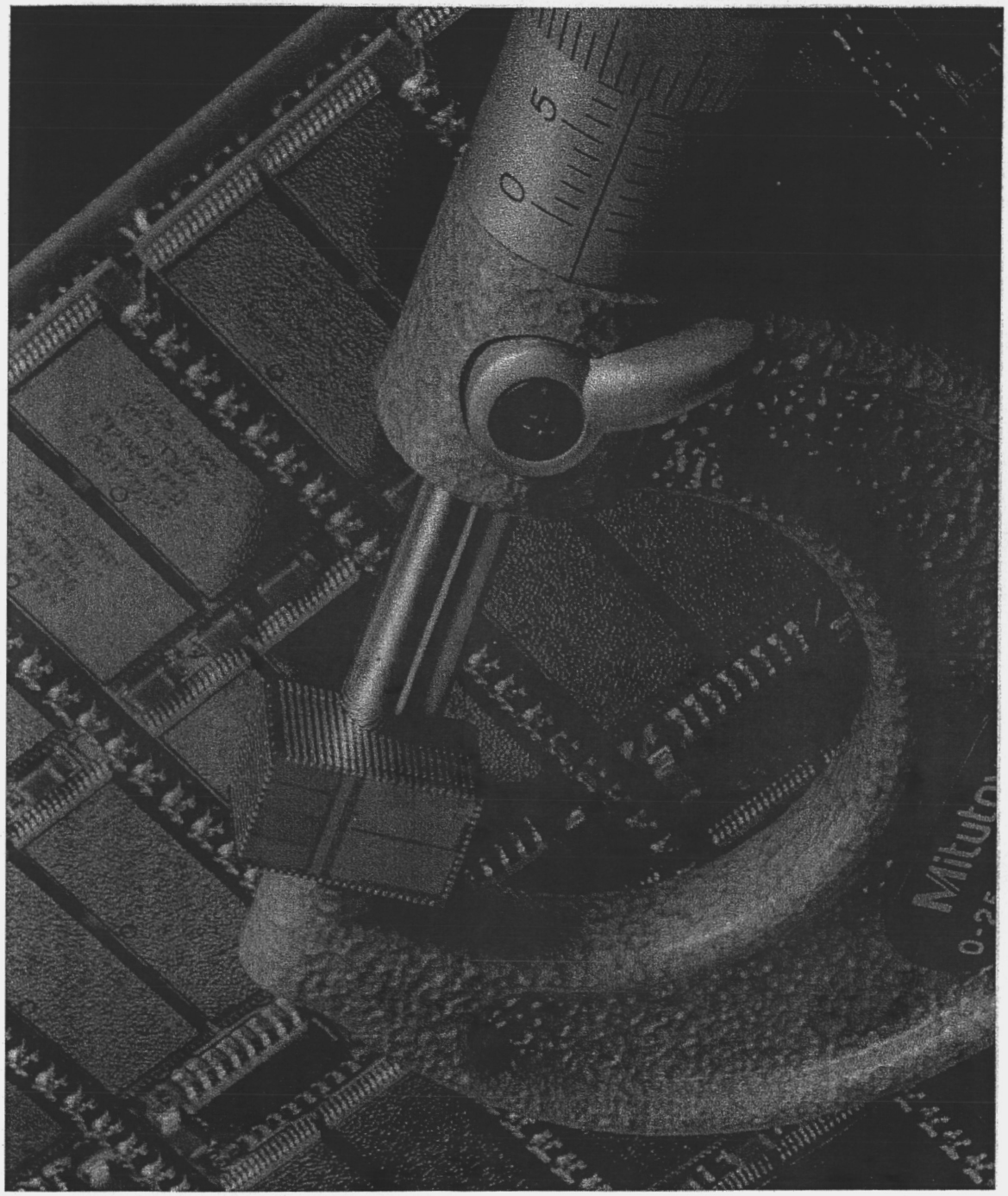


Figure 21. Irvine Sensors Memory Cube. (Courtesy of Irvine Sensors)

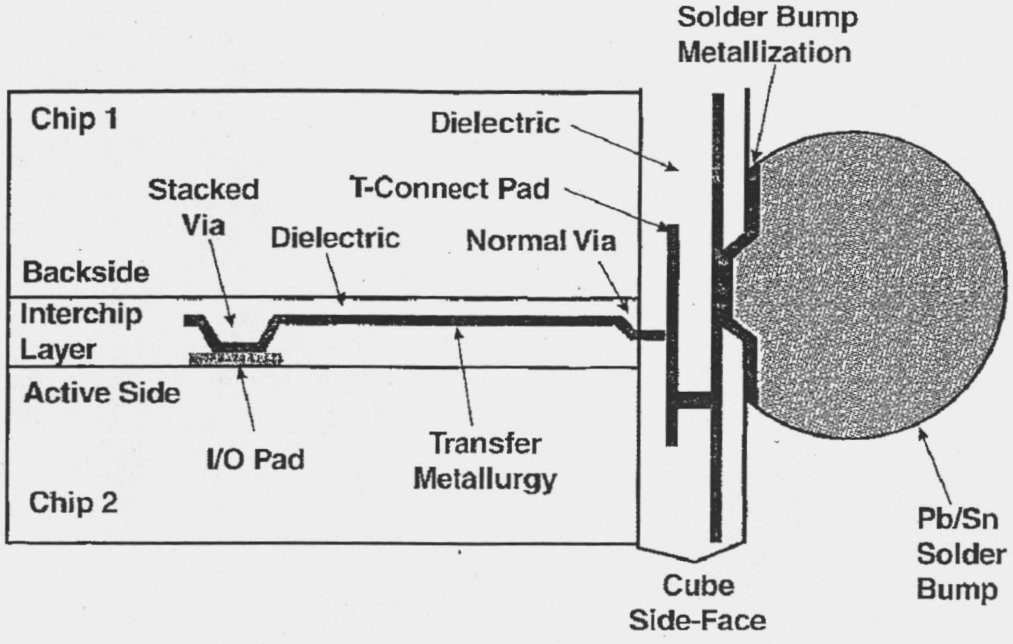



Figure 22. Use of a Thick Polyimide Layer for I/O Redistribution and 'Gluing" of Die into a Cube. [Caterer.pdf]

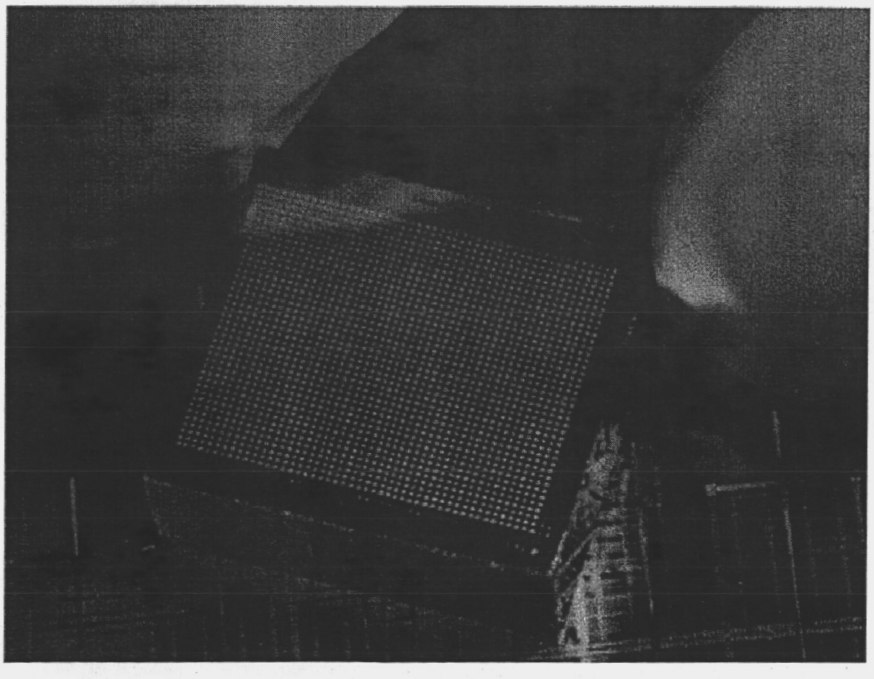


Figure 23. Example of Memory Cube [Caterer.pdf]

Lea, in conjunction with Irvine Sensors, developed a 3-D massively parallel processor die stack [Lea.pdf]. The die I/O were re-routed to two sides of the die using thin film gold metallization. The wafers were then thinned and diced. Using adhesive, the die were laminated between top and bottom ceramic substrates (AlN) (Figure 24).Two sides of the

cube were polished, exposing the re-routed I/O. The edges were then metallized. The ceramic cap chip provided routing for wire bond pads – wire bonds are used to electrically interconnect from the cube to the package or substrate (Figure 24).

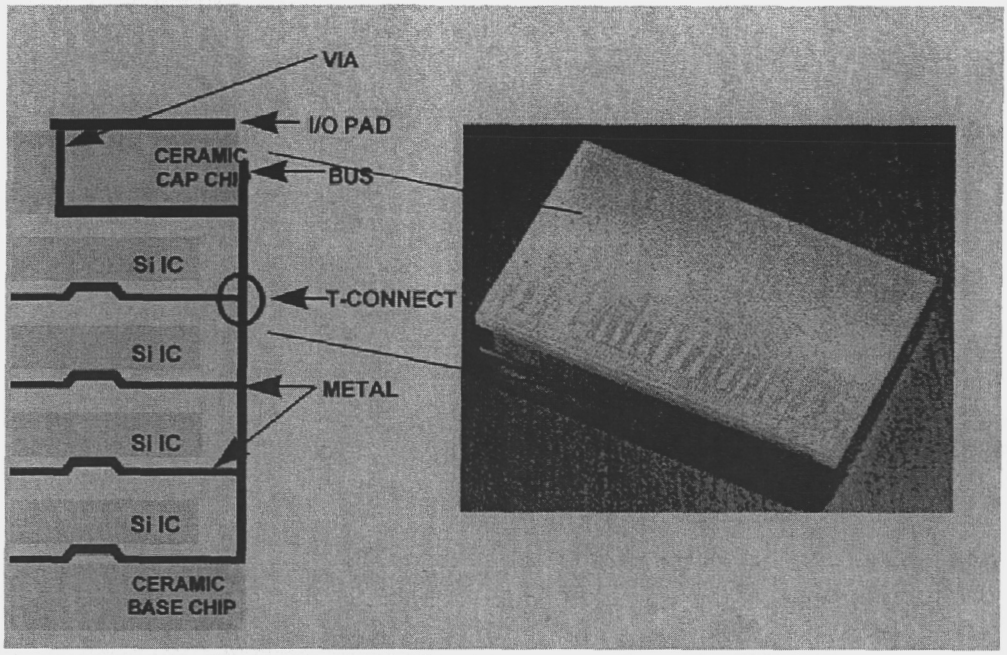



Figure 24. Example of Die Stack between Ceramic Chips. [Lea.pdf]

Irvine Sensors develop the NEO stack technology to allow stacking of different size die and multiple die per layer [Gann-2.pdf, Gann-3.pdf]. A single die layer is illustrated in Figure 25, while a two die layer is shown in Figure 26. Known good die are stud bumped using a gold wire bonder. The die are then arrayed and potted to create a NEO wafer. Polyimide and thin film metallization are patterned on the surface of the NEO wafer. The NEO wafer is then diced. A thin layer of epoxy is used to bond the stack of NEO die as illustrated in Figure 27. The stack is then ground on the edges to expose the perimeter traces and metallized providing provide z-axis interconnections. A completed cube is shown in Figure 28.

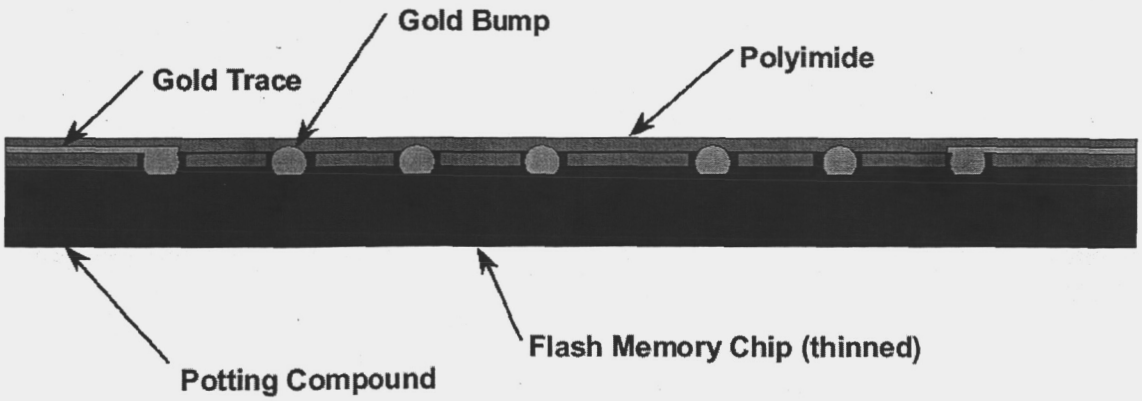



Figure 25. Single Die Irvine Sensors NEO Layer. [ Gann-3.pdf ]

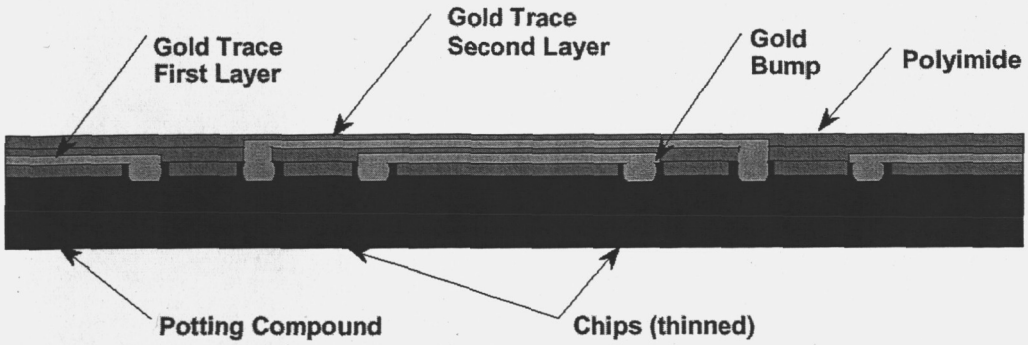



Figure 26. Two Die Irvine Sensors NEO Layer. [Gann-3.pdf]

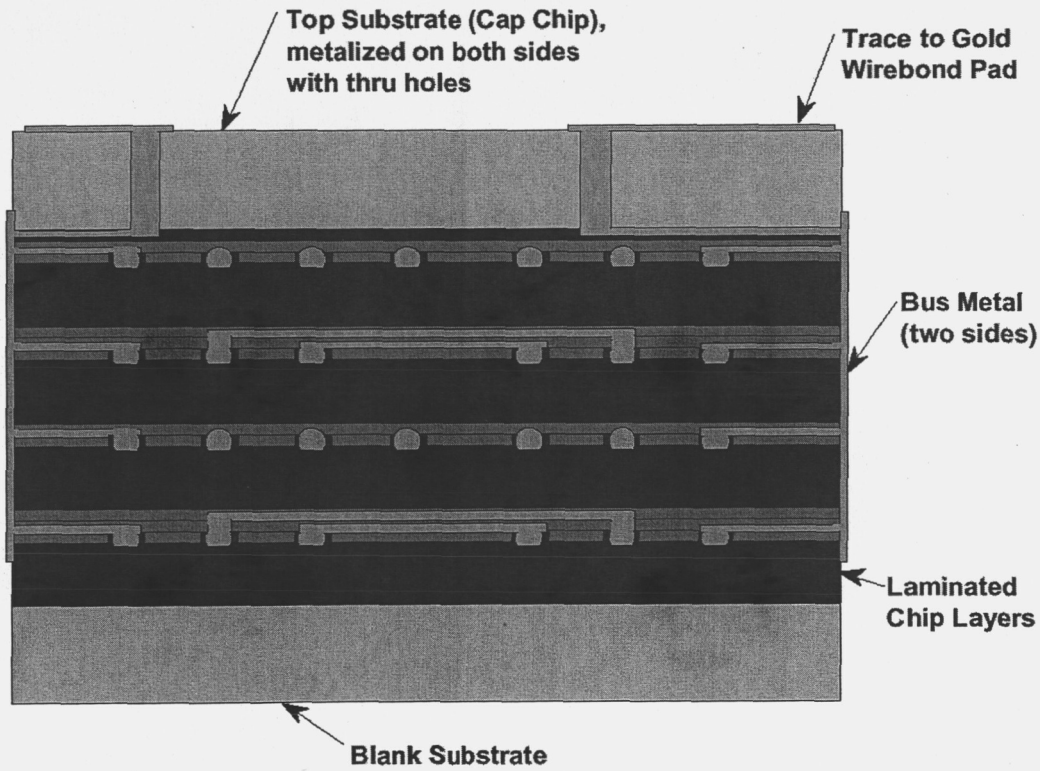



Figure 27. Cube Created from Stack of NEO Layers. [Gann-3.pdf]

Val, et al. has developed a die stacking technology based on wire bonding die to a flex substrate [Val-2.pdf]. Perimeter probe pads on the substrate facilitate die testing and burn-in. Tested die are then stacked and molded into a cube. A diamond saw is used to cut the edges of the cube, exposing the wire bond wires. Electroless Cu/Ni/Au is used to metallize the edges of the cube. Patterning of the edge metallization is accomplished with a laser. The process is illustrated in Figure 29.

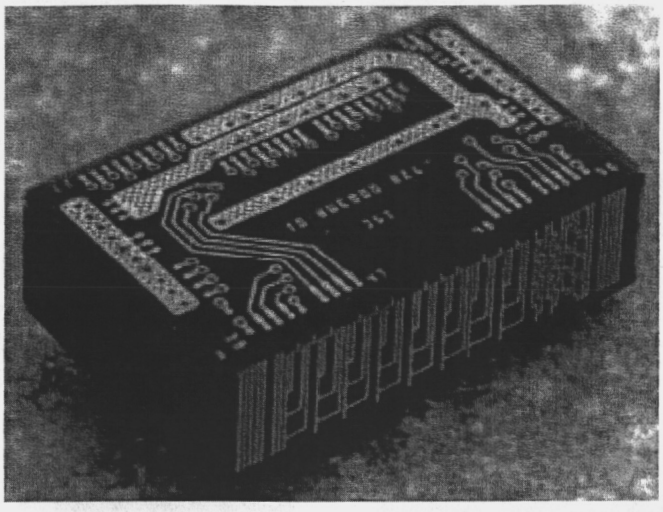


Figure 28. Example of Irvine Sensors Flash Memory Cube. [Gann-3.pdf]

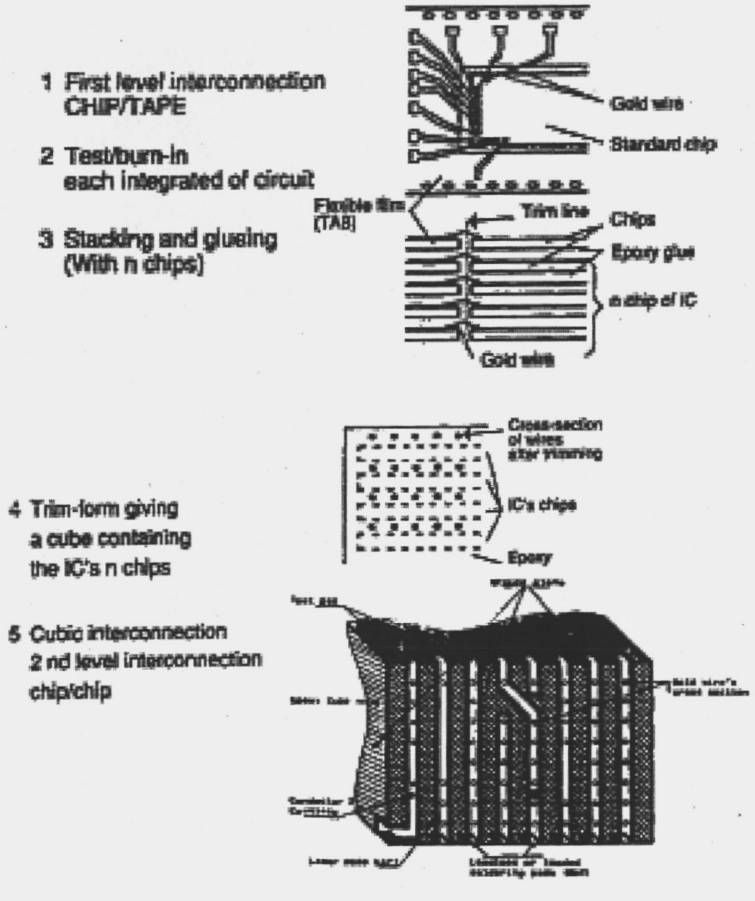



Figure 29. Illustration of 3D Cube Fabrication Process. [Val-2.pdf]

Die stacking to create cubes can package many die in a small volume, but requires significant post die processing. The primary die stacking technology in volume production today involves stacking two or more thinned die and wire bonding them into a package (TSOP, BGA, CSP). Examples of this type of die stacking are illustrated in Figures 30-32. In Figure 30, tooling is used to allow double-sided die attach and wire bonding prior to transfer molding in a TSOP [Nakanishi.pdf]. Figure 31 illustrates an alternate approach, where two lead frames are used. After wire bonding, the two lead frames are joined by either Ag-Sn solder or Ag-to-Ag thermocompression bonding [Cho.pdf]. Figure 32 illustrates die attach of one die on the surface of another and wire bonding to a common substrate prior to transfer molding [Kada.pdf]. Combining flip chip and wire bond assembly as illustrated in Figure 33 allows a high I/O count area array die to be flip chip assembled as the bottom die in a two die stack [Carson.pdf]. Alternately, if the flip chip die is smaller than the wire bond die, a redistribution layer can be processed on the wire bond die and the smaller die flip chip attached on top of the wire bond die [Dufresne.pdf]. Figure 34 illustrates combining stacked and non-stacked die in a common multichip package [ Amkor.pdf ].

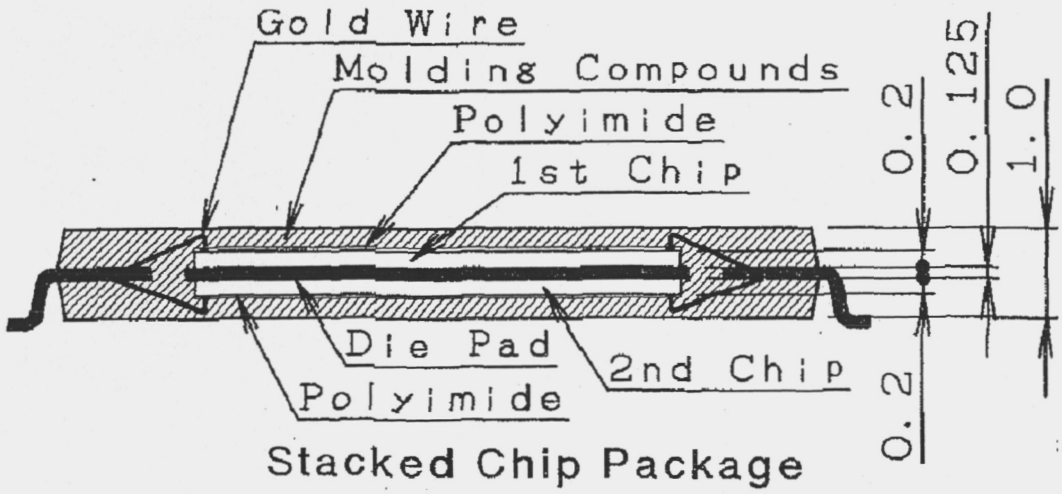
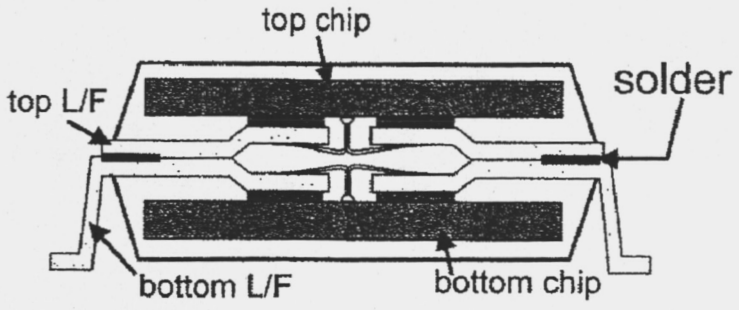
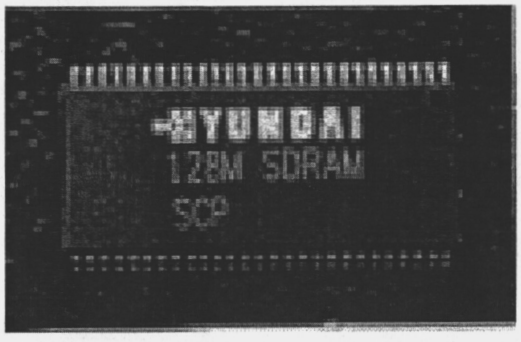



Figure 30. Two Die TSOP, Single Lead Frame. [Nakanishi.pdf]



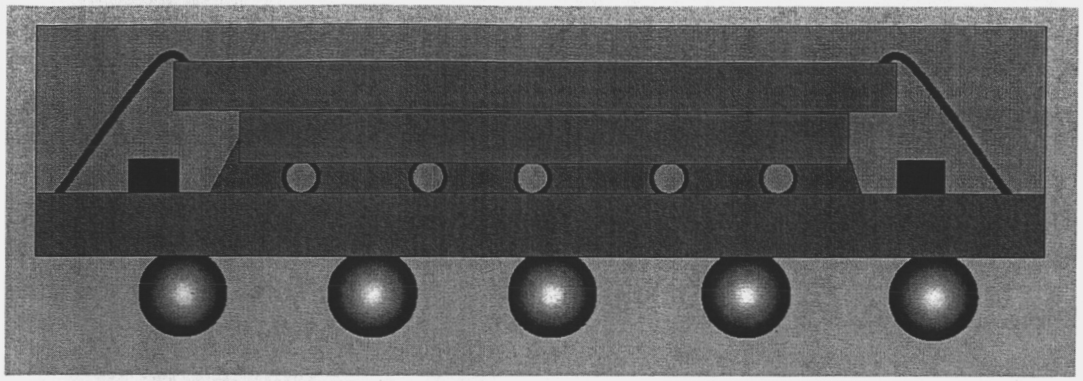

(a)



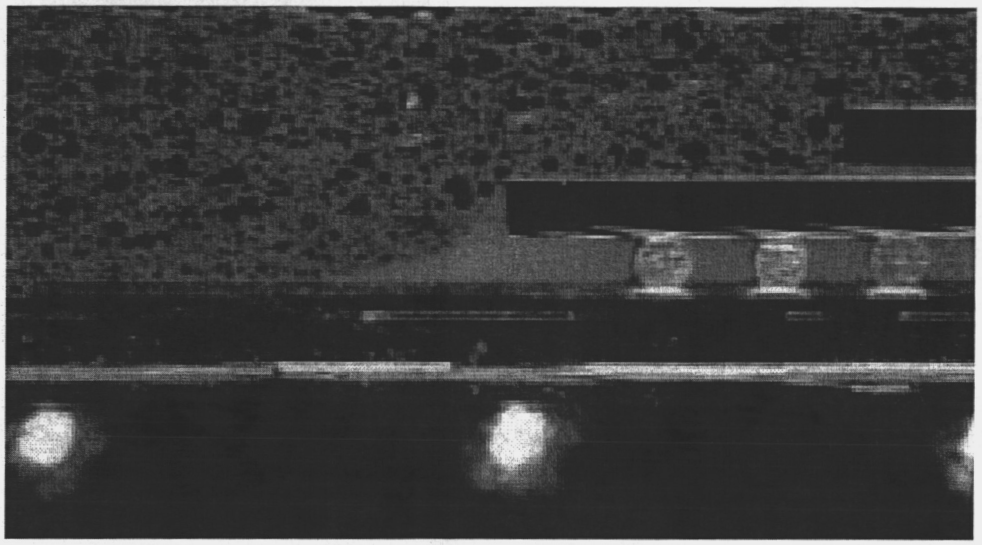

(b)

Figure 31. Two Die TSOP – Two Lead Frames, Common Transfer Mold. [Cho.pdf].


Figure 32. Illustration of Two Die CSP with Rigid Laminate Substrate. [Kada.pdf]



(a)



(b)

Figure 33. Illustration (a) and Cross Section (b) of Wire Bond plus Flip Chip Two Die Assembly. [Carson.pdf]

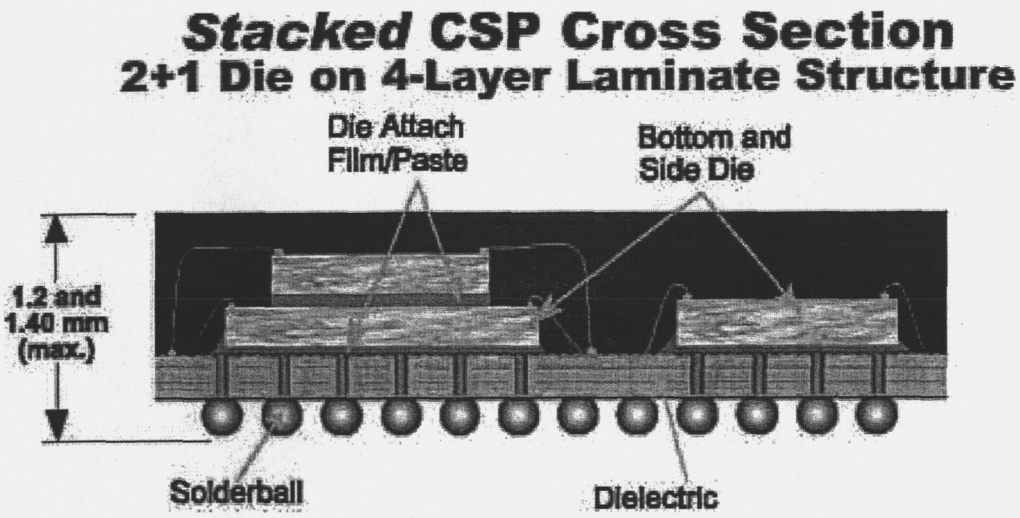



Figure 34. Multiple Die (Single and Stacked) in Package. [Amkor.pdf]

The key technologies for die stacking are wafer thinning, thin die handling and advanced wire bonding. Mechanical, Chemical-Mechanical, Chemical, Plasma and combinations of these are used to thin silicon die. 100μm thick die are commonly used today and 75μm and thinner die are beginning to be used. However, Sempek has identified issues with refresh interval degradation with thinned memory die [Sempek.pdf]. The exact cause has not been identified, but there is concern over contamination from the Chemical-Mechanical Polishing (CMP) slurry. According to Sempek, other potential issues with thinning include single bit failures, reverse tunneling effects, and punch through. Lépinois [Lépinois.pdf] has studied the effect of thinning on the electrical characteristics of transistors. The performance of bipolar transistors is only affected in marginal cases when dislocations are introduced by the thinning process. The effect was only observed at low currents level, below normal operation levels. The only effect observed in MOS devices was self heating in power MOS transistors due to the replacement of Si with polymer, increasing the thermal resistance for heat transfer by conduction.

Advances in wire bond loop control have made complex wire bonding of stacked die possible (Figure 35). To maintain low loop heights, reverse wire bonding ($1^{st}$ wire bond on package substrate, $2^{nd}$ wire bond on die) is often used. To avoid shorting of the wire to the Si die surface, a stud bump is bonded to the I/O pad and the $2^{nd}$ wire bond is made to the top of the stud as shown in Figures 35 and 36. Wire bonding to overhanging, thinned die has also been developed (Figure 37). Wire sweep during transfer molding must be considered in die stacks with a high density of closely spaced wire bonds.

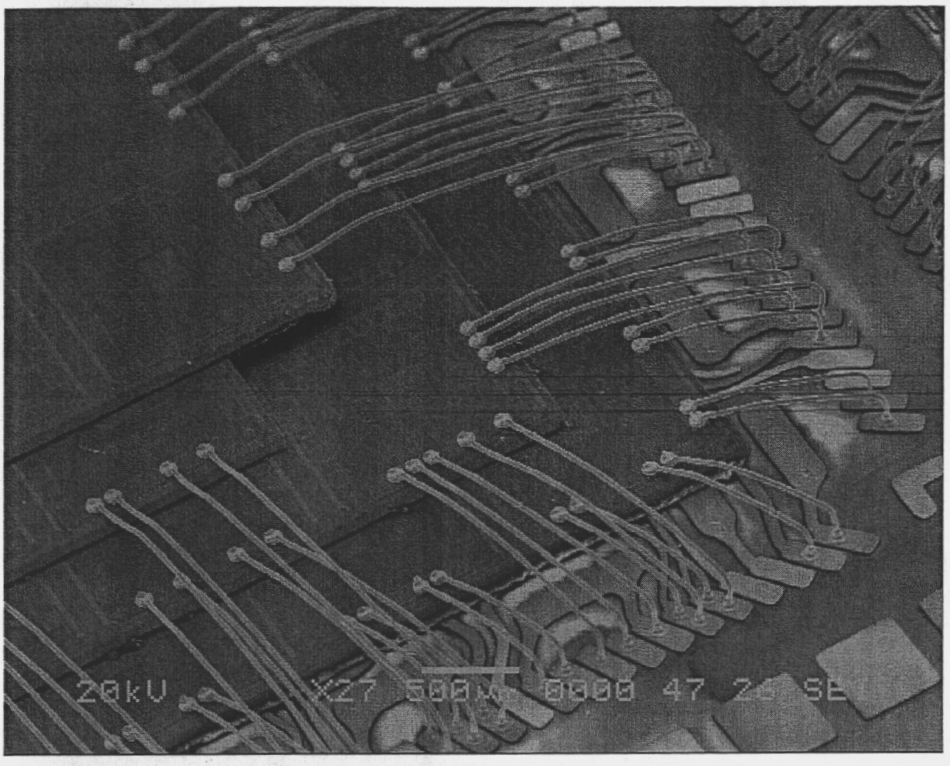



Figure 35. Example of Wire Bonding of Stacked Die. (Courtesy of Amkor)

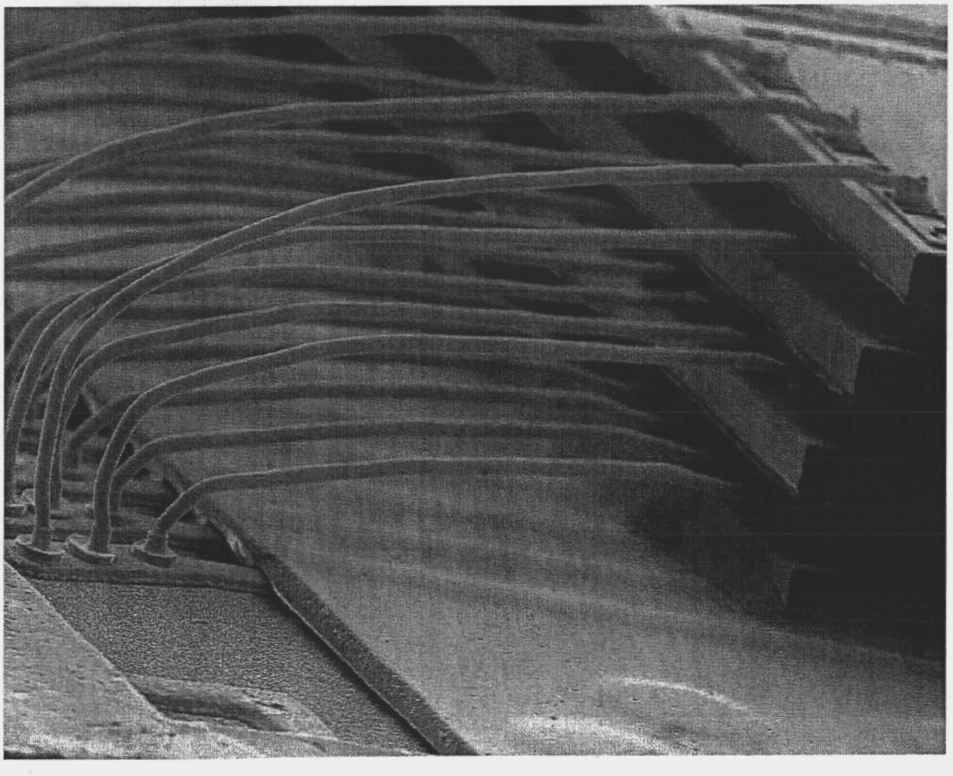


Figure 36. Example of Reverse Wire Bonding with Au Studs on the Die. (Courtesy of Amkor)

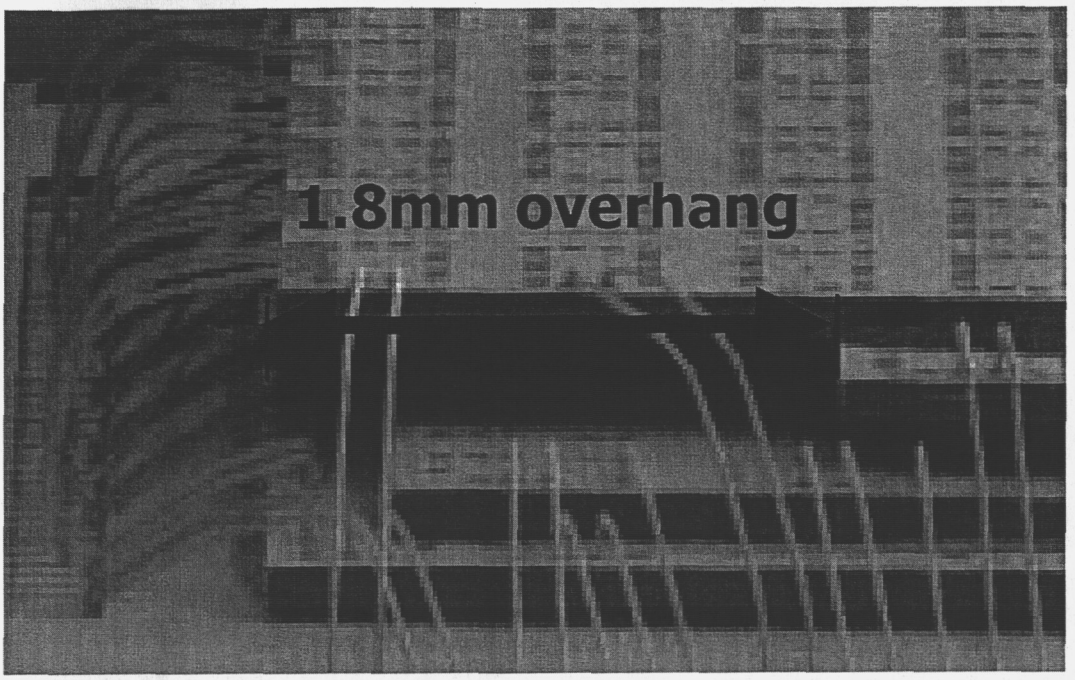



Figure 37. Wire Bonding to 100μm Thick, Overhanging Die. [Carson.pdf]

Epoxies and silicone adhesives are used for die attachment. Key characteristics of die attach adhesives for stacked die include:

1. Non-abrasive to avoid damage to die passivation (polyimide, silicon nitride, etc.)
2. Low stress – increasingly important for low-k dielectrics used in the multilevel metal systems of advanced semiconductors to reduce on-chip propagation delays. These low-k dielectrics have lower mechanical strength than traditional dielectric materials.
3. High thermal conductivity to transfer heat through the stack to the substrate or lead frame.
4. Controlled bond line thickness to maintain a controlled spacing between die. Controlled bond line thickness is important for electrical isolation, stack thickness control and to prevent wire bond damage.

When assembling same size die, silicon spacer die are often used (Figure 38) to maintain adequate spacing between die to prevent damage to the wire bonds [Carson.pdf]. In same size die assemblies, each die must be placed and wire bonded before the next die is placed.

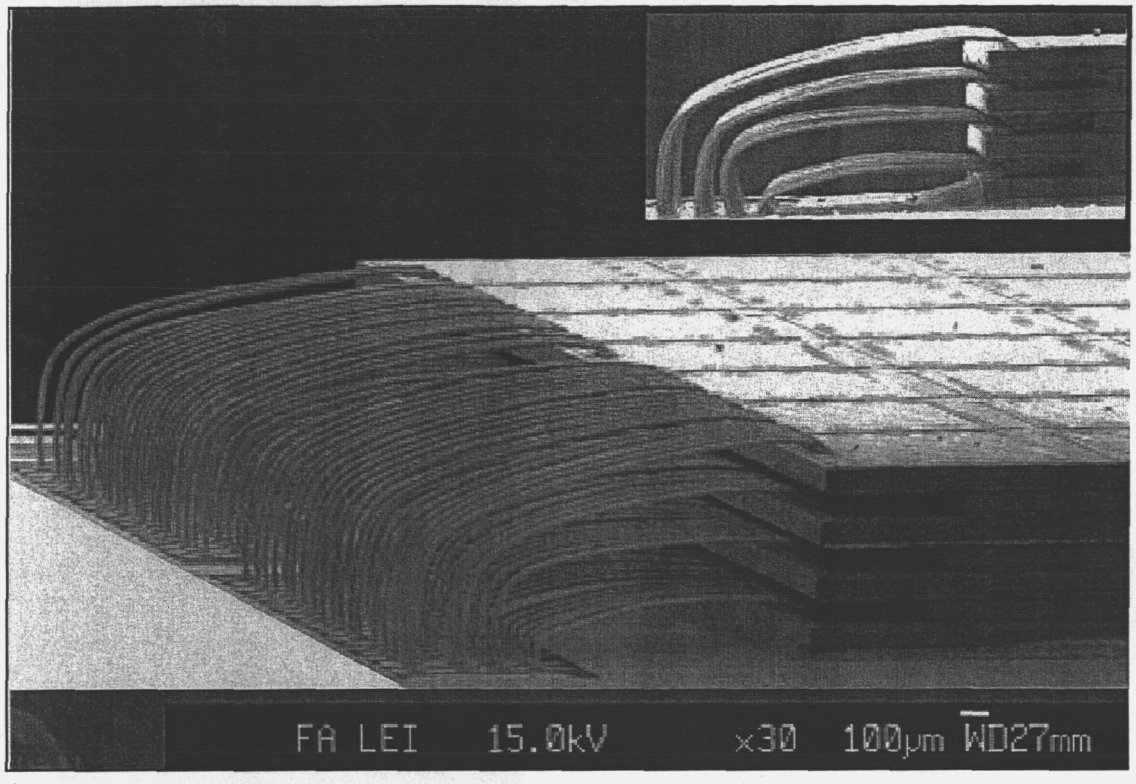



Figure 38. Example of Same-Size Die Stacked Using Silicon Spacers. [Carson.pdf]

An alternate die stacking option is to assemble die to a flex substrate and then fold the flex to create a 3-D stack. Auburn University [Johnson.doc], Tessera [Solberg-3.pdf] and the IST-99-10205 Project FLEX-Si 'Ultra-thin Packaging Solutions Using Thin Silicon' funded by the European Commission have pioneered folded flex technology [Balde.doc, Harder.doc, Kallmayer.doc]. The work by Johnson and by the European Program focused on flip chip based die assembly, while Tessera has extended their µBGA single chip packaging technology to create folded flex assemblies.

Figure 39 shows the original four die stack demonstrated by Johnson, et al. [Johnson.doc]. The four die were assembled to the flex substrate using a patterned isotropic conductive adhesive. Once assembled, the flex substrate was cut and folded to create the 3-D stack. Non-conductive adhesive preform sheets was used to adhere the layers of the folded stack.

The Tessera µZ® 3-D folded three die stack technology is show in Figure 40 [Solberg-1.pdf]. Figure 41 shows the substrate details. Tessera uses either the wire bonding (Figure 42) or the lead bonding (Figure 43) technology developed for their µBGA® single chip packaging technology. In the wire bond approach, wire bonds are from the die surface to the pads on the flex substrate through a window opened into the flex substrate. After wire bonding, the wire bonds are encapsulated. For the lead bond technology, the leads are patterned as part of the flex substrate. The polyimide is then etched away, creating the bond window. The bond windows in the substrate are shown in Figure 45. Using a conventional wire bonder with a modified bonding tool, force is applied to the lead

causing it to break in the narrow region. Ultrasonic energy is then used to bond the lead to the die bond pad.

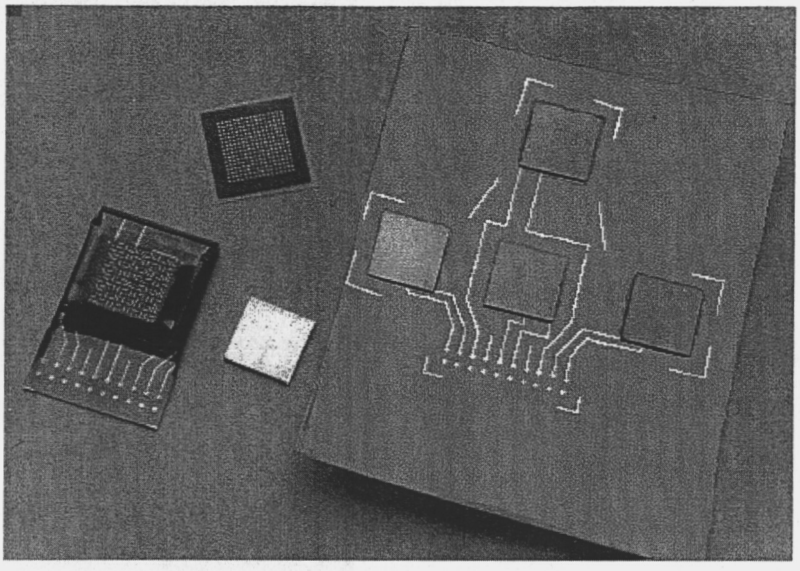


Figure 39. Folded Stack 3-D Assembly. [Johnson.doc]

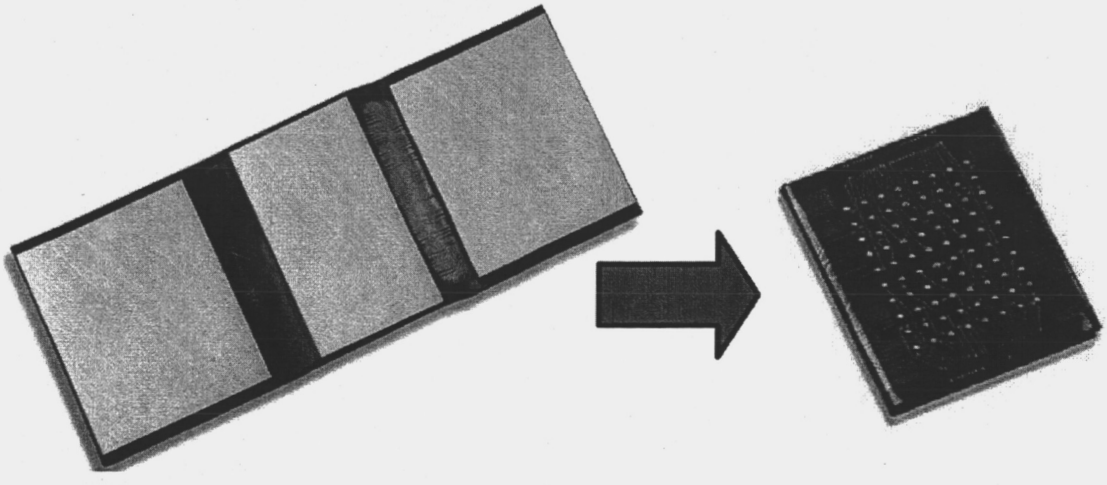


Figure 40. Example of Tessera 3 Die μZ® Technology with Two FLASH Die and One SRAM Die. [Solberg-1.pdf]

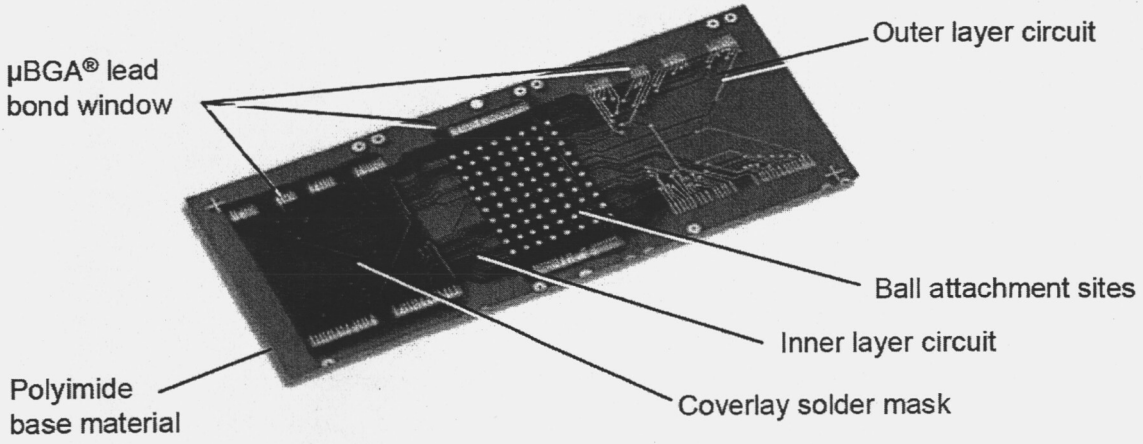



Figure 41. Substrate Details for Tessera 3 Die µZ® Technology. [Solberg-1.pdf]

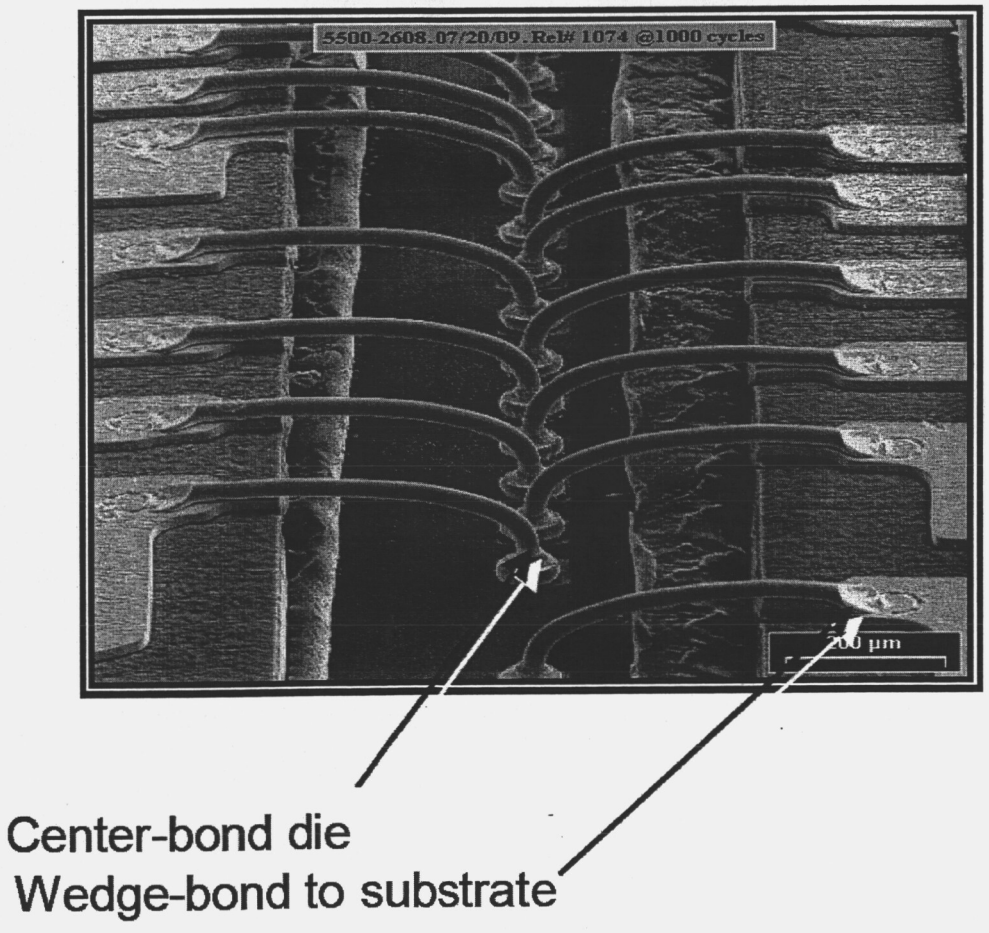



Figure 42. Example of Wire Bonded Tessera Die-to-Substrate Interconnection. [Solberg-3.pdf]

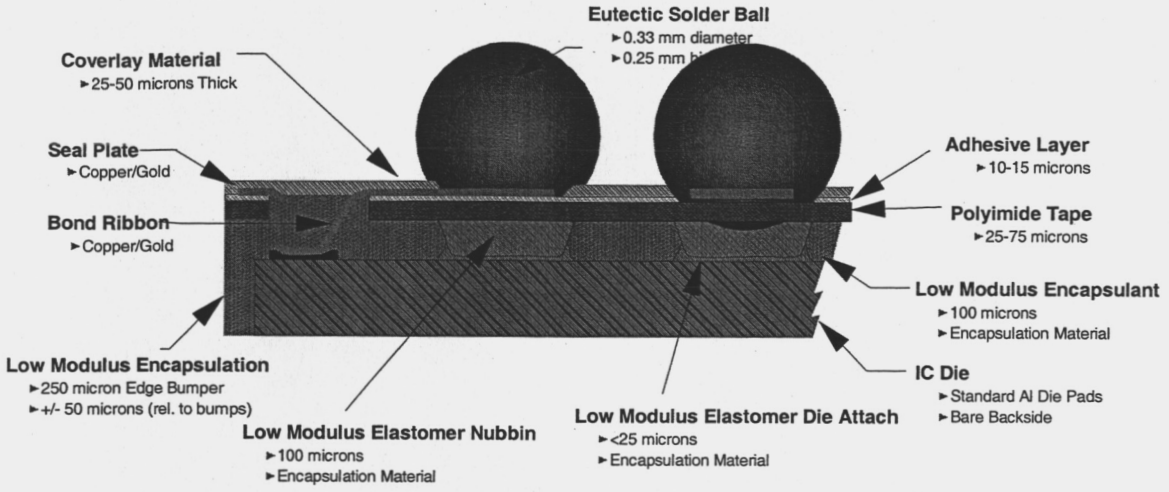



Figure 43. Illustration of Tessera μBGA® Single Chip Packaging Showing Lead Bond from Substrate to Die. [Solberg-4.pdf]

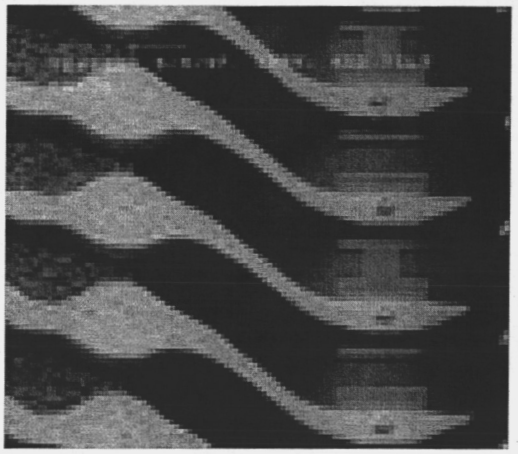


Figure 45. Lead Bonds from Flex Substrate Through Lead Bond Window to Die Pads. [Solberg-3.pdf]

A primary advantage of folded flex technology is the ability to use area array die. However, the chip-to-chip routing is effectively 2-D. Furthermore, two or more metal layer flex substrates are expensive and the number of suppliers is limited.

For the ultimate in die stacking, thru-silicon vias can be fabricated to provide electrical paths through the silicon die. With I/O pads on both sides of the die, the die can be stacked and interconnected without wire bonds. Using a thin (1.5μm) Sn2.5Ag cap on the Cu thru-vias, the electrical interconnects from die to die are formed on a heated flip chip bonder by converting the Cu and Sn into $Cu_3Sn$ intermetallic [Takahashi.pdf]. The process is illustrated in Figure 46. Vacuum encapsulation is used to underfill between the die in the stack. A four die stack is shown in Figure 47 [Umemoto.pdf]. This process requires significant backend wafer processing. It is possible for high volume devices that

benefit from 3-D stacking such as memory, that thru-silicon vias will be integrated into the memory design and wafer fabrication in the future.

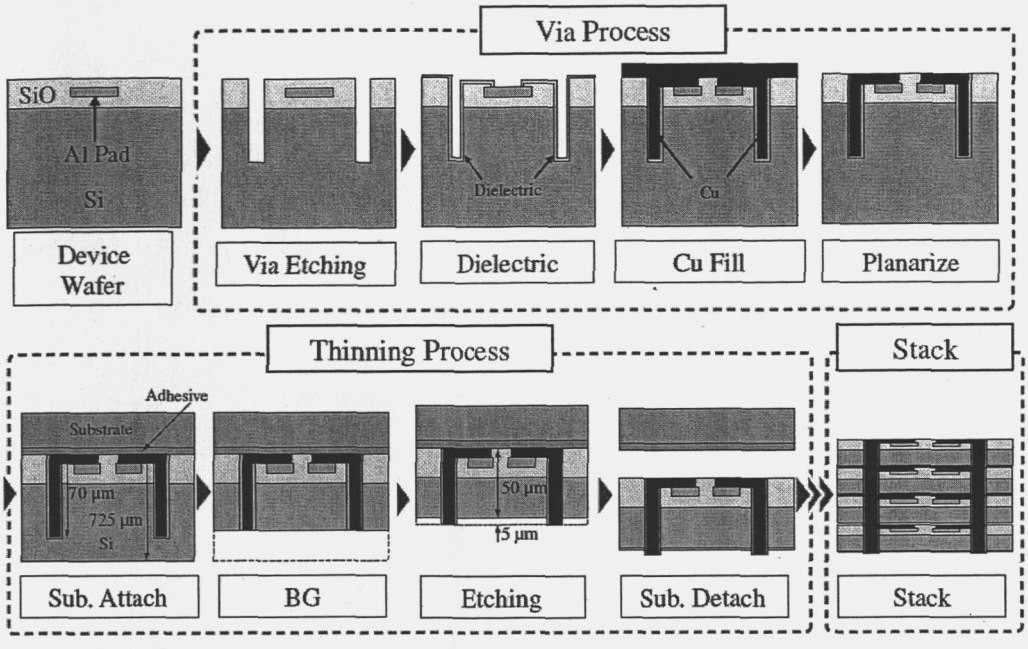



Figure 46. Process for Die Stacking with Thru-Silicon Vias. [Takahashi.pdf]

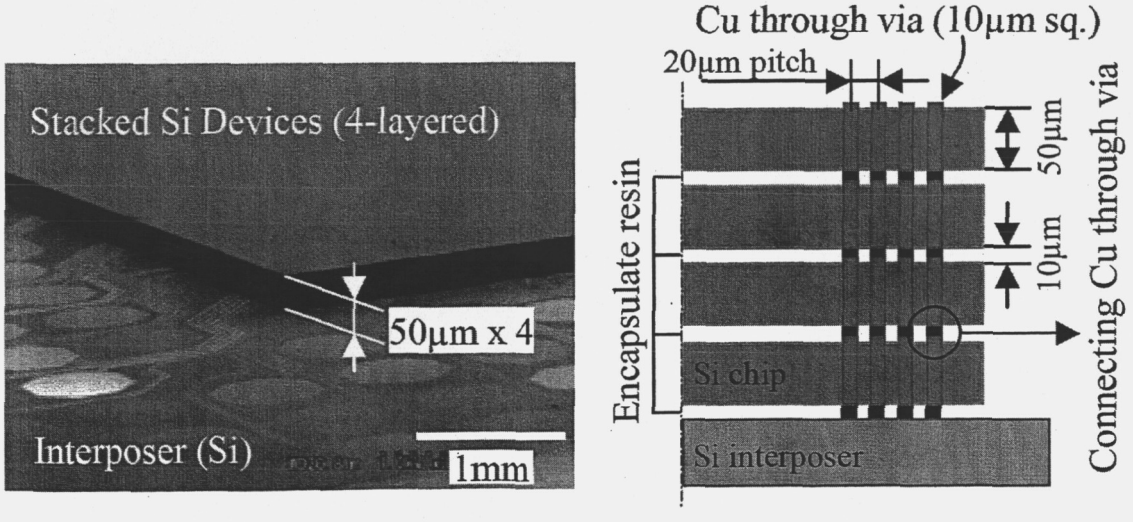



Figure 47. Four Die Stack with Thru-Silicon Vias. [Umemoto.pdf]

Benefits of Die Stacking: Die stacking provides a significant decrease in size and weight and reduces next level assembly costs. It is particularly well suited for memory or memory in combination with a single microprocessor or digital signal processing chip. Two die wire bonded stacks are in high volume production for cell phone and other

portable products and the die count is trending upward. With die thinning, stacked die packages are no thicker than traditional single chip packages. Die stacking reduces signal path length compared to individual packages.

Limitations of Die Stacking: The key limitations to die stacking are die yield and thermal dissipation. The thermal performance is limited by the package (BGA, CSP, etc.). The total power dissipation for all die in the stack is limited to the power dissipation limit of the same package with a single die. In the case of one low power die and one high power die, the lower power die may actually run hotter due to heat transfer from the higher power die [Awad.pdf]. A microfluidic-thermoelectric cooler has been proposed to remove the heat from stacked die [Furmanczyk.pdf]. CVD diamond heatspreader layers have also been investigated [Ozguz.pdf]. Thermal management is becoming a critical factor in electronics packaging for both single and stacked die.

Acceptable package level yield relies on either high die yield or testing for known good die. Rework within the package is not practical. To address this yield issue, Package-in-Package (PiP) has been introduced [Carson.pdf]. As illustrated in Figure 48, the concept is to integrate a pre-assembled and pre-test package into a 3D stack. Wire bonds are used to connect the top package to the base package substrate.

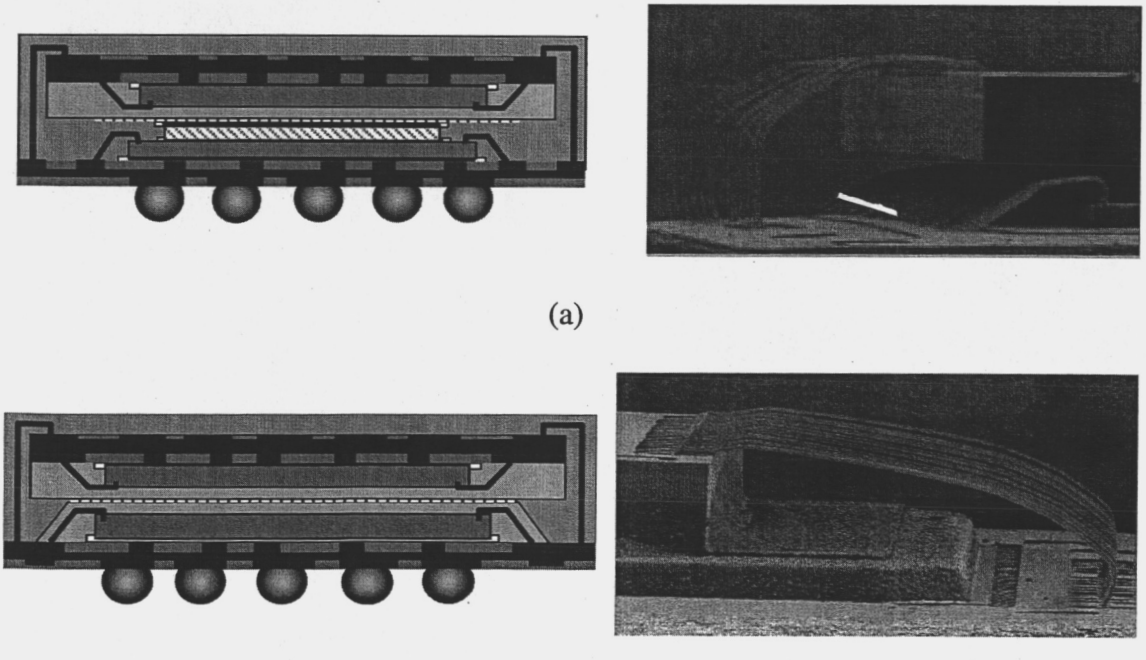


Figure 48. Illustration and Photograph of Package-in-Package Technology. [Carson.pdf]

Tessera has developed a PiP approach using a foldable flex tab integrated into the fabrication of one package to provide interconnection to the second package. The concept is illustrated in Figure 49 [Tessera.htm].

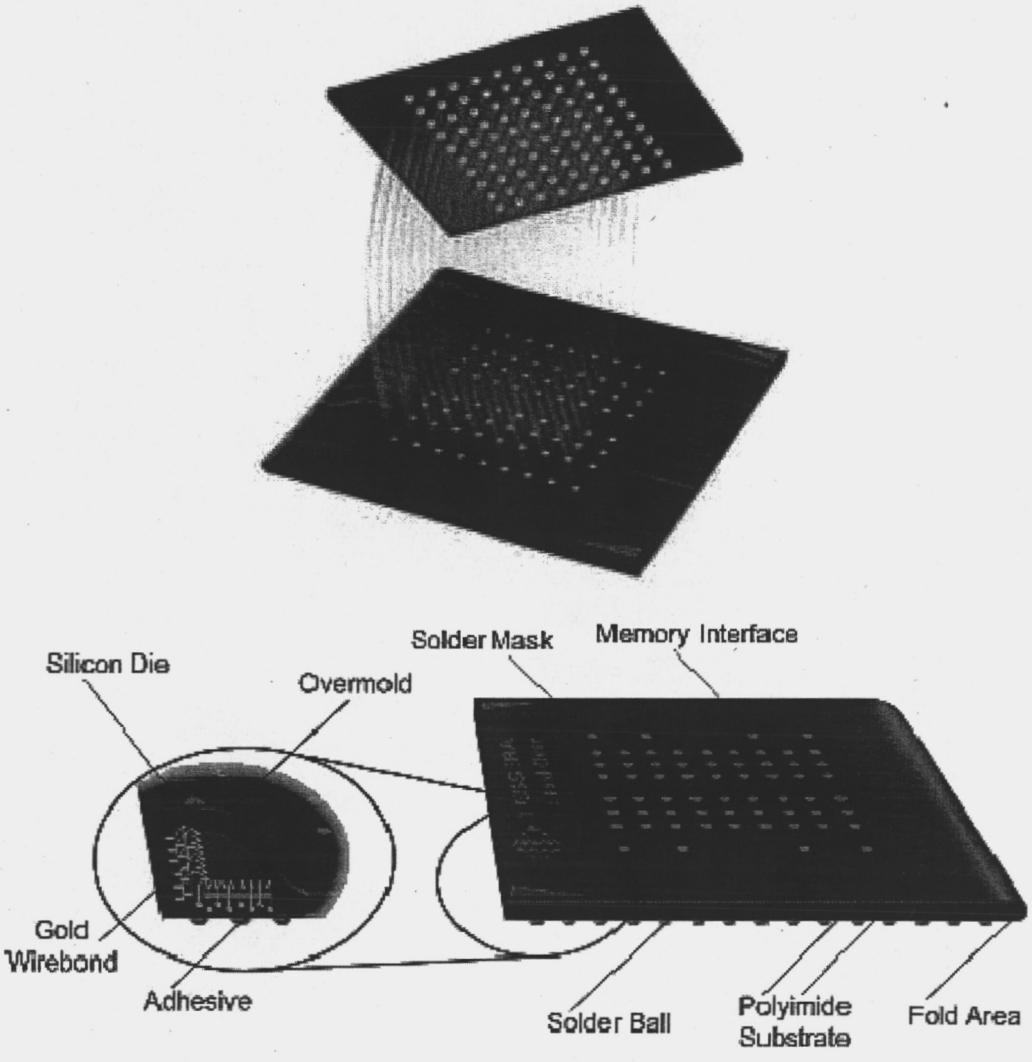



Figure 49. Tessera Fold-Over μZ Technology. [Tessera.htm]

Reliability: The reliability of the stacked die packages is similar to that of the equivalent single die package. Nakanishi has reported similar reliability for two die TSOPs [Nakanishi.pdf]. Fukui, et al. [Fukui.pdf] has shown similar thermal cycle reliability for two and three die stack (wire bonded) CSPs (Figure 50). The 3-D stacking technology developed by Val and now manufactured by 3D-Plus has been through extensive reliability testing [Barrett.pdf].

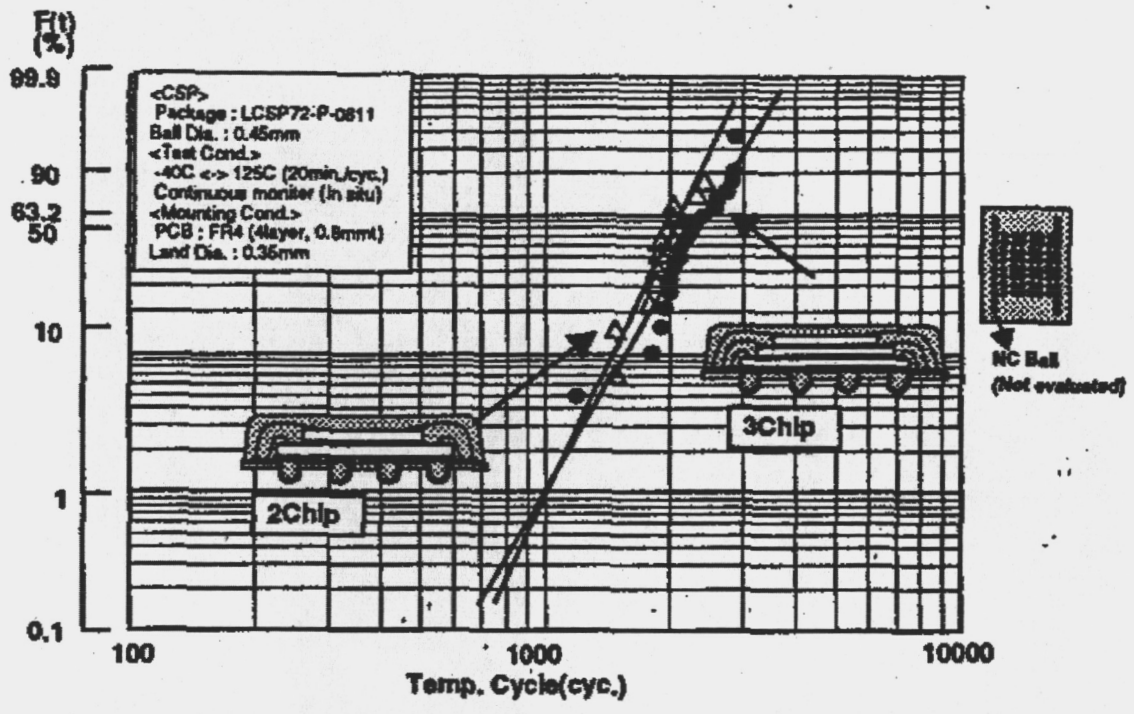



Figure 50. Thermal Cycle (-40°C to +125°C) Reliability for 2 and 3 Die Stacks. [Fukui.pdf]

The Amkor data sheet [Amkor.pdf] reliability data for stacked (wire bond) CSPs is:

Package Level
- Moisture Resistance Testing JEDEC Level 3 @260°C
- Additional Test Data at [(30°C/85%RH/96hrs)+260]x2or3
- Temp Cycle -55/+125°C, 1000 cycles
- Unbiased Autoclave/PCT 121°C/100% RH/2atm, 168 hours
- Temp/Humidity 85°C/85%RH/1000 hours
- High Temp Storage 150°C, 1000 hours

Board Level
- Thermal Cycle -40/+125°C, 4000 cycles

Technology Readiness Level Assessment: The die cube technology developed by Irvine Sensors has been used to build solid state data recorders that have flown on NASA missions. Thus this technology readiness level of this technology is TRL 7-8. The 3D-Plus die stacking technology has been used in space applications. The stacked die in package (wire bond and/or flip chip) has comparable reliability to commercial single die CSPs. As single chip CSPs have been evaluated by NASA, but have not flown, the technology is at TRL 3-4. Folded flex and Package-in-Package technologies are also at TRL 3 as test data for space environment conditions and requirements has not been generated.

### 3-D Multichip Modules

With significant funding from DARPA in the 1990's, there was significant development in 2-D multichip modules. A convergence of chip-on-board, cofired ceramic and deposited multilayer thin film technologies lead to MCM-Laminate (MCM-L, Figure 51), MCM-Ceramic or Glass/Cermic (MCM-C, Figure 52) and MCM-Deposited (MCM-D, Figure 53) approaches respectively. There were also combinations of these, i.e. thin film layers deposited on top of cofired ceramics (MCM-C/D), etc. These technologies provided a high density of 2-D interconnections and with the elimination of individual chip packages a high density of die, again in a 2-D array. These technologies are in use today, with few chip MCM-L dominating the commercial market. The need for known good die and the associated yield favors few chip modules. Increasing the number of die per module decreases overall module yield unless the certainty of know good die increases. MCM-C and MCM-D are typically hermetic packages and have been used for space applications. The Jet Propulsion Laboratory is developing a chip-on-board (MCM-L) assembly for the Mars Science Laboratory.

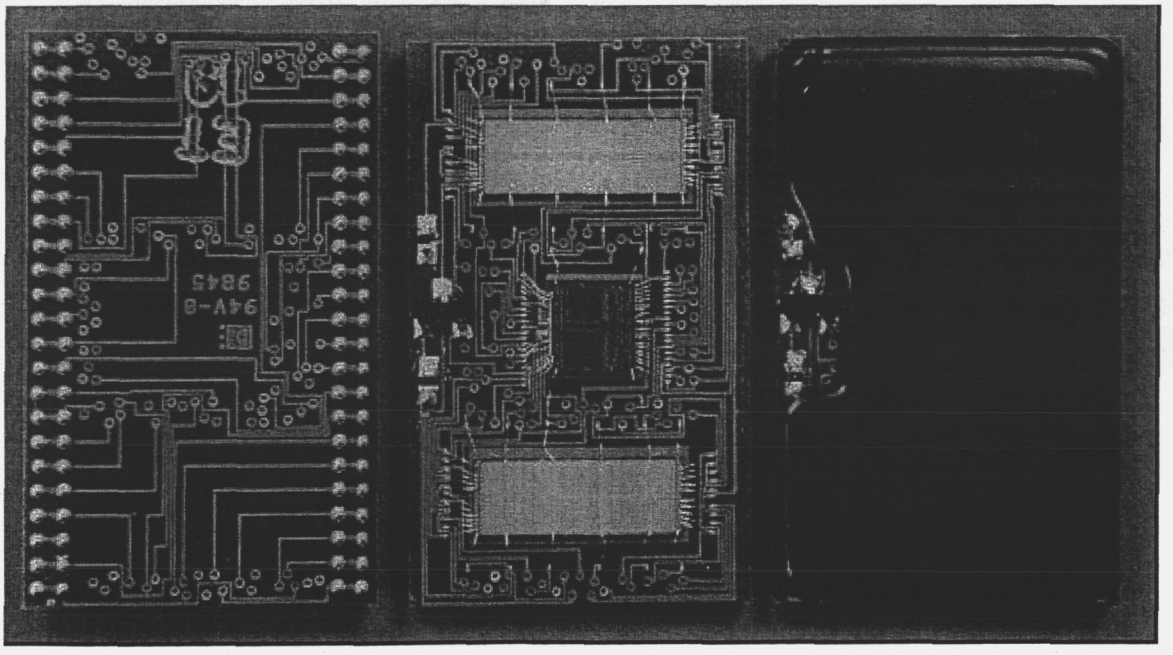


Figure 51. Example of MCM-L Fabricated at Auburn University. Left: Bottom side of MCM-L, Center: Top side before encapsulation, Right: Top side after Encapsulation.

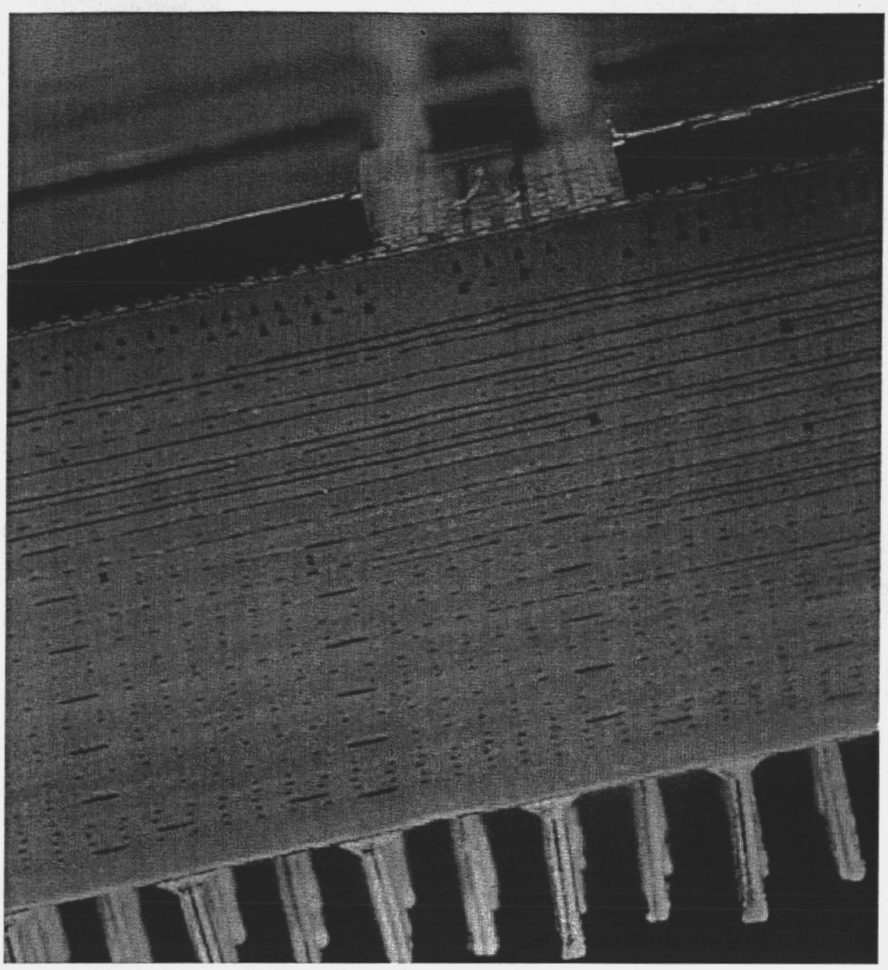


Figure 52. Cross Section of IBM Cofired Glass-Ceramic Multichip Module Used for Mainframe Computer Applications.

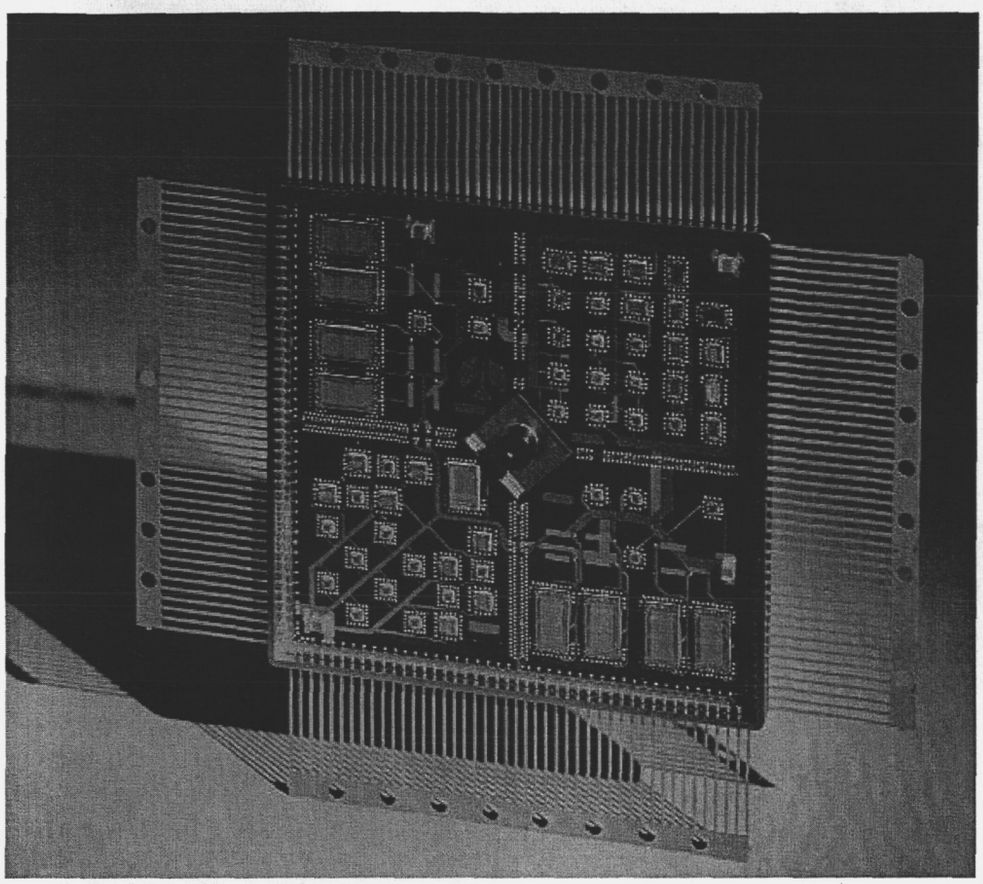


Figure 53. Example of Avionics MCM-D from Rockwell Collins.

MCM-L, MCM-C, and MCM-D are all examples of chips last, i.e. the interconnect substrate is fabricated and then the die attached to complete the module. Auburn University, General Electric and Lockheed-Martin have each developed 'chip first' technologies. The original General Electric concept is illustrated in Figure 54 [Saia.pdf]. The process flow is illustrated in Figure 55 [Daum.pdf]. Die were placed in machined cavities in a ceramic substrate. A polyimide film (Kapton) was overlaid and adhered to the surface of the die and the ceramic. Vias were laser drilled down to the I/O pads on the die. Thin film metallization was used to interconnect the die. The film, laser drilling and metallization steps were repeated to create multilayer interconnections. General Electric has developed several variations of this basic approach for different applications. The challenge of known good die is more critical in the 'chips first' approach, since rework is limited.

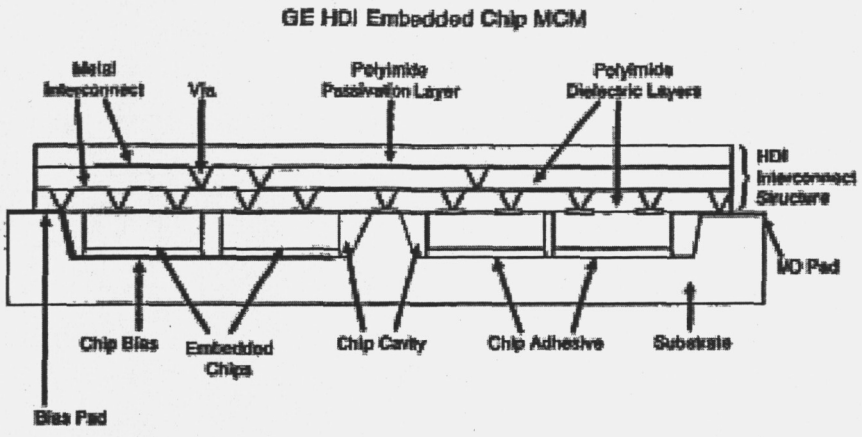



Figure 54. Illustration of GE HDI-MCM 'Chips-First' Approach. [Saia.pdf]

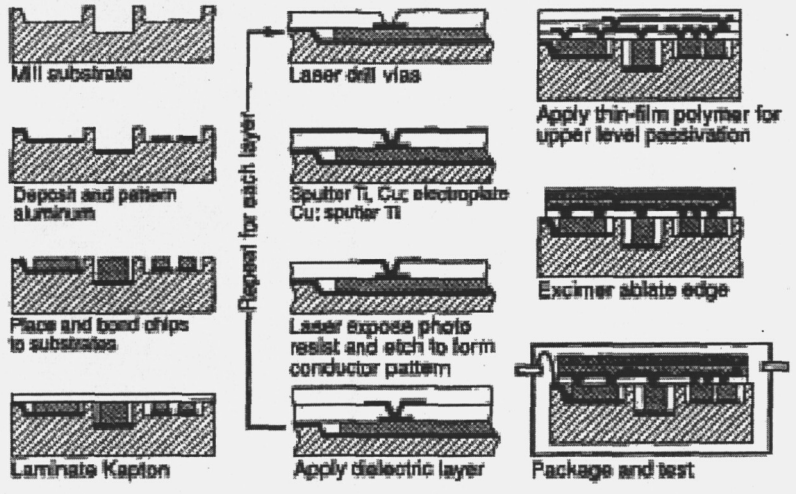



Figure 55. General Electric 'Chips First' MCM Technology Process Flow. [Daum.pdf]

A number of approaches to 3-D multichip modules have been developed. Jensen, et al developed a two-sided MCM-C module (Figures 56 and 57) [Jensen.pdf]. Note the MCM also contains stacked die. The ability to process vias through the layers of the ceramic substrate provided front-to-back electrical interconnections. Clarke, et al. also developed a two-sided MCM-C using a 23 metal layer cofired aluminum nitride substrate [Clarke.pdf].

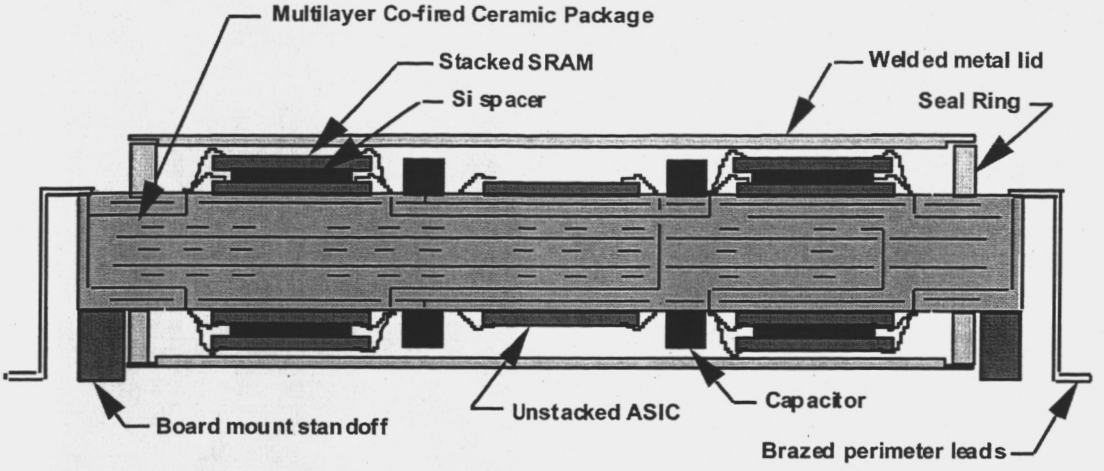



Figure 56. Illustration of Two-Sided MCM-C. [Jensen.pdf]

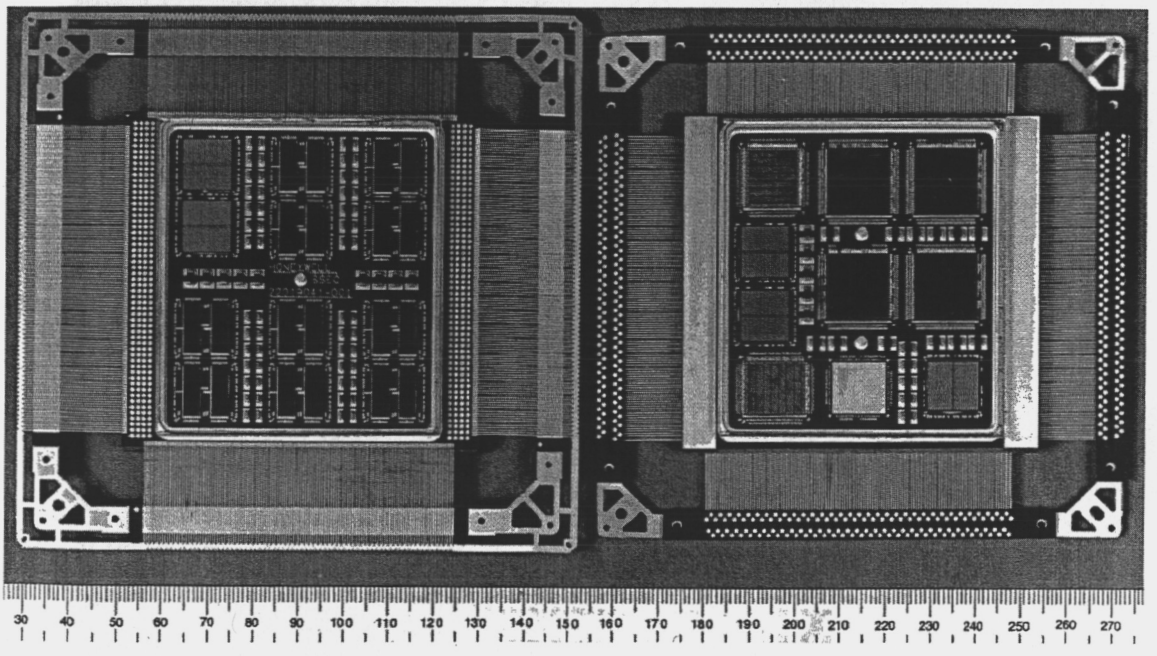


Figure 57. Front and Back Views of 32-Bit Computer MCM. [Jensen.pdf]

Ceramic and laminate based multichip module technologies provide direct front-to-back electrical interconnections, allowing double sided assemblies. However, this only results in two active levels of devices, a limited 3-D capability. A number of approaches have been developed to create 3-D MCMs with multiple active layers. These are primarily based on edge connections. One pioneer in this field is 3D-Pus (BUC, France). The process sequence is shown in Figure 58 [Val-1.pdf]. The circuit is partitioned into layers. Each layer is designed onto a flex epoxy/glass substrate and may contain passive components, packaged chips, chip-and-wire, flip chip die and other elements. An example substrate layer is shown in Figure 59 [Alexandre.pdf]. "Flying leads" are created in the substrates (Figure 59 and 60) for interconnections that must interconnect between

layers. Once the substrate layers are fabricated and the devices are assembled, they are electrically tested. Pads are designed along the perimeter of the substrate to facilitate electrical testing. The individual layers are then stacked and molded into a cube. The cube is sawn to expose the "flying leads" as shown in Figure 61. Plating (Ni/Au) and laser patterning are used to define the electrical interconnections along the cube edge between layers (Figure 62). The Vertical InteGration for Opto and Radio (VIGOR) subsystems illustrated in Figure 63 were developed based on the 3D-Plus technology with funding from the European Union 3-D Integration Project [Alexandre.pdf]. The project focused on printed circuit board dielectric materials and "flying lead" formation, molding compound materials and edge metallizations and patterning technologies.

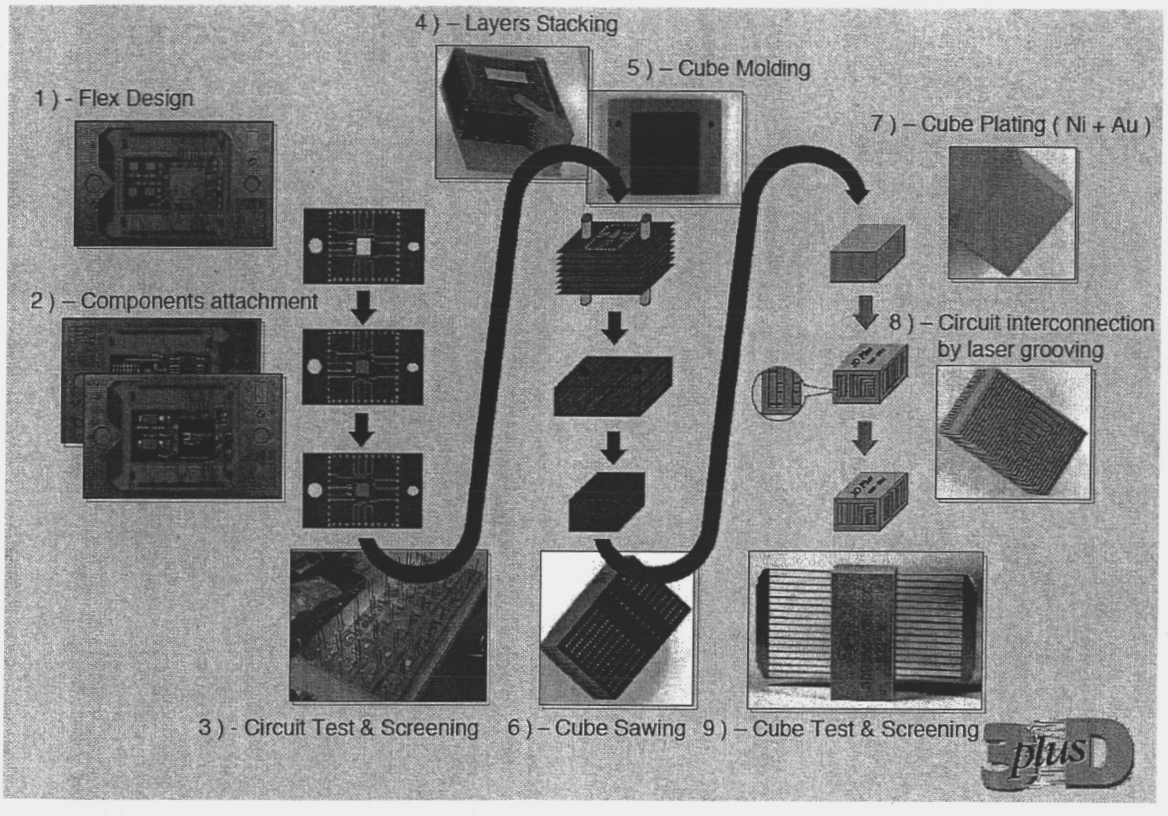



Figure 58. 3D-Plus Process Flow. [Val-1.pdf]

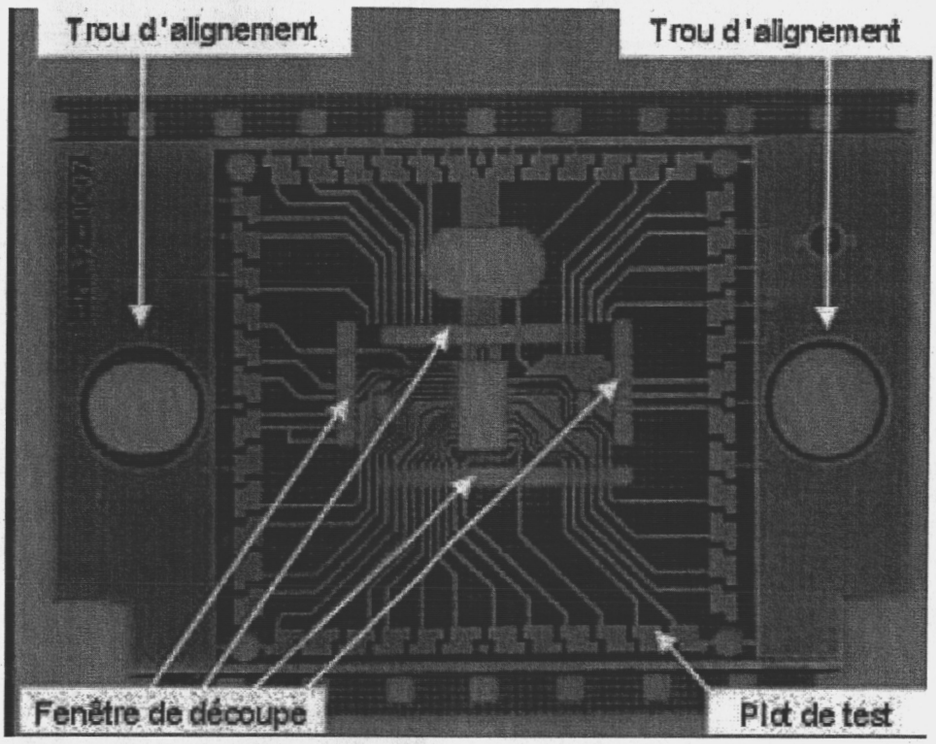



Figure 59. Example Substrate for 3D-Plus Cube. [Alexandre.pdf]

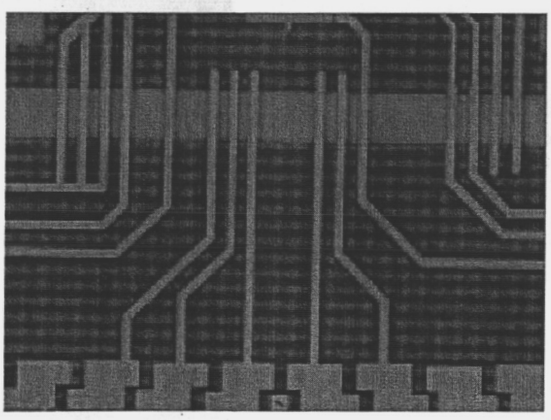


Figure 60. Close-up of "Flying Leads". [Alexandre.pdf]

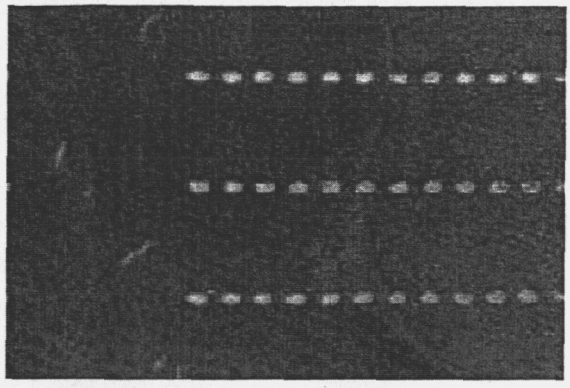


Figure 61. Exposed Copper "Flying Leads" after Sawing. [Alexandre.pdf]

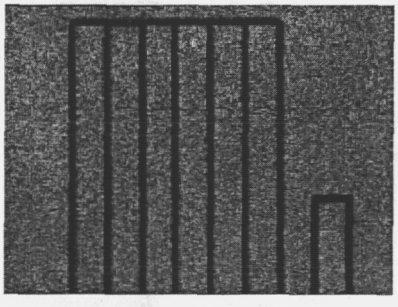


Figure 62. Ni/Au Metallized Cube with laser Patterning. [Alexandre.pdf]

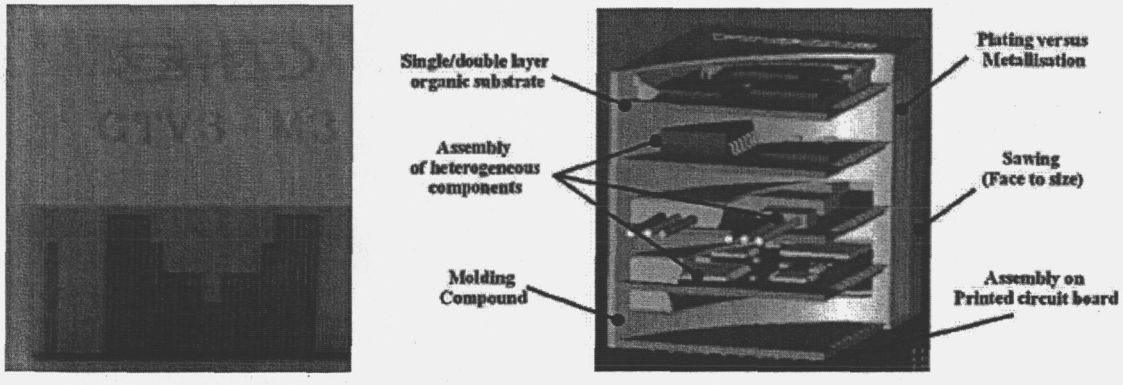
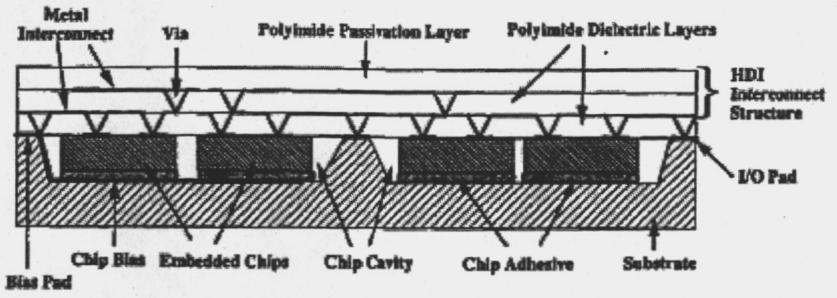
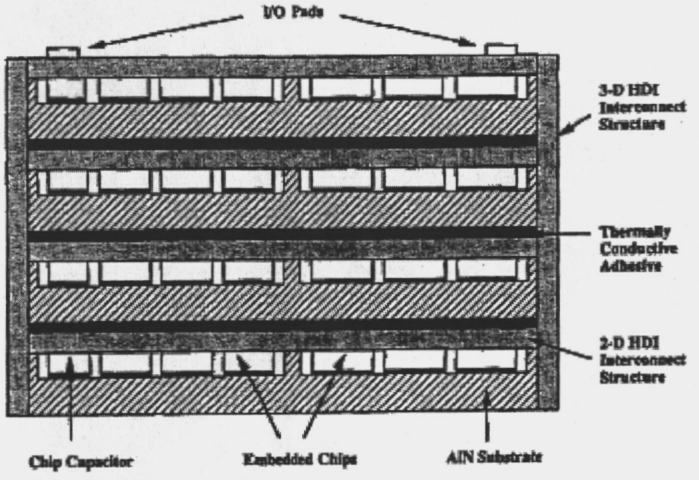



Figure 63. Example and Illustration of VIGOR Test Vehicle. [Alexandre.pdf]

General Electric has developed a 3D MCM technology based on their 'chips first' HDI MCM technology [Wojnarowski.pdf]. The concept is illustrated in Figure 64 and the process sequence is illustrated in Figure 65. Polyimide film with laser based vias and copper interconnections are used to make cube edge connections between layers. A close-up is shown in Figure 66. An example 3D MCM is shown in Figure 67 [Fillion.pdf].




. (a) Single HDI-MCM Layer




(b) HDI-MCM Stack

Figure 64. Illustration of GE 3D MCM Stack. [Wojnarowski.pdf]

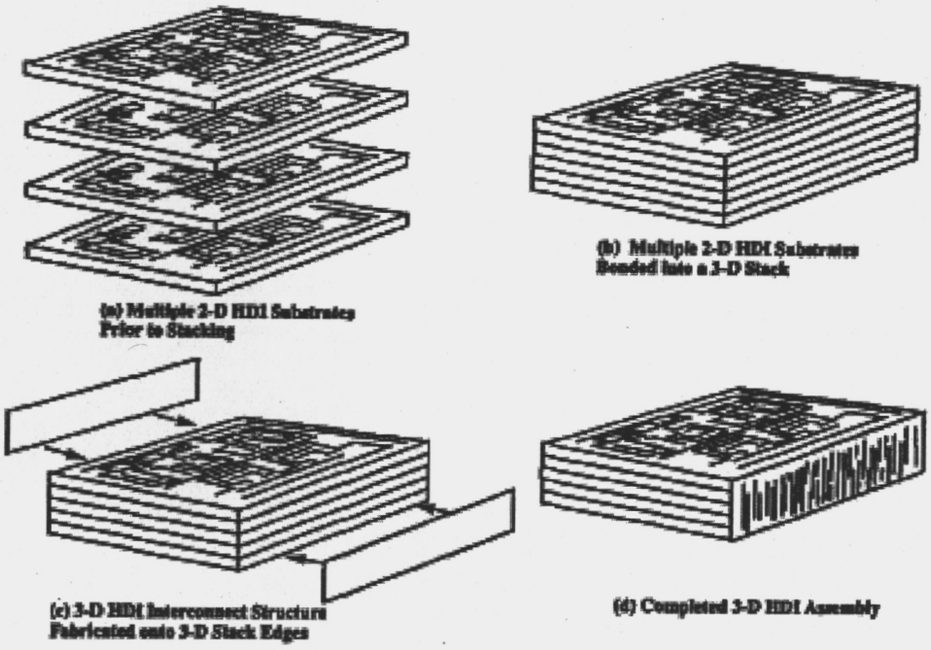



Figure 65. GE 3D Stack Process Sequence. [Wojnarowski.pdf]

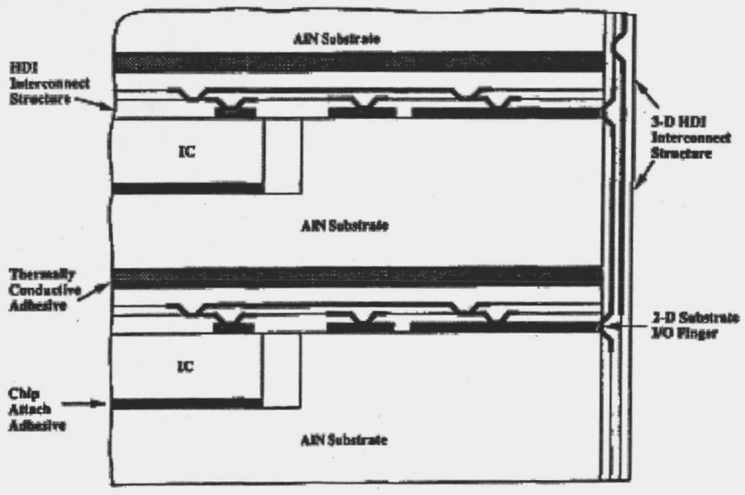



Figure 66. Close-up of 3D Edge Connection. [Wojnarowski.pdf]

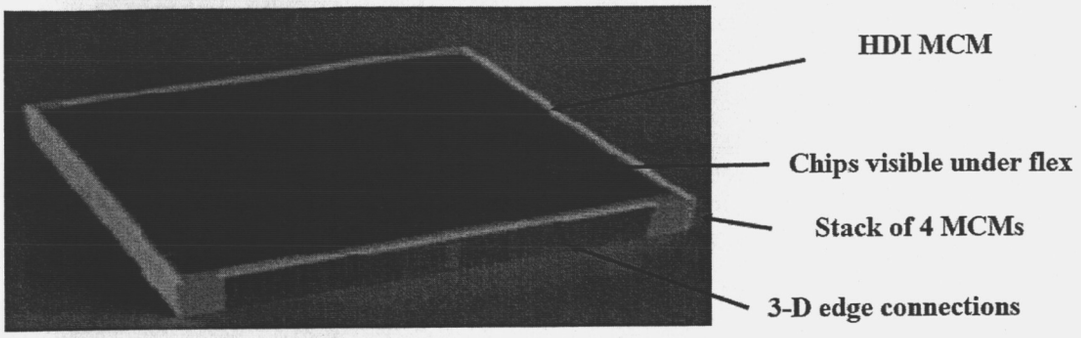



Figure 67. Four Layer GE 3D MCM. [Fillion.pdf]

Pienimaa, et al. has developed a 3-D MCM stacking approach using Sn/Ag plated plastic balls around the perimeter of the MCMs to interconnect between MCMs [Pienimaa.pdf]. The process sequence is illustrated in Figure 68.

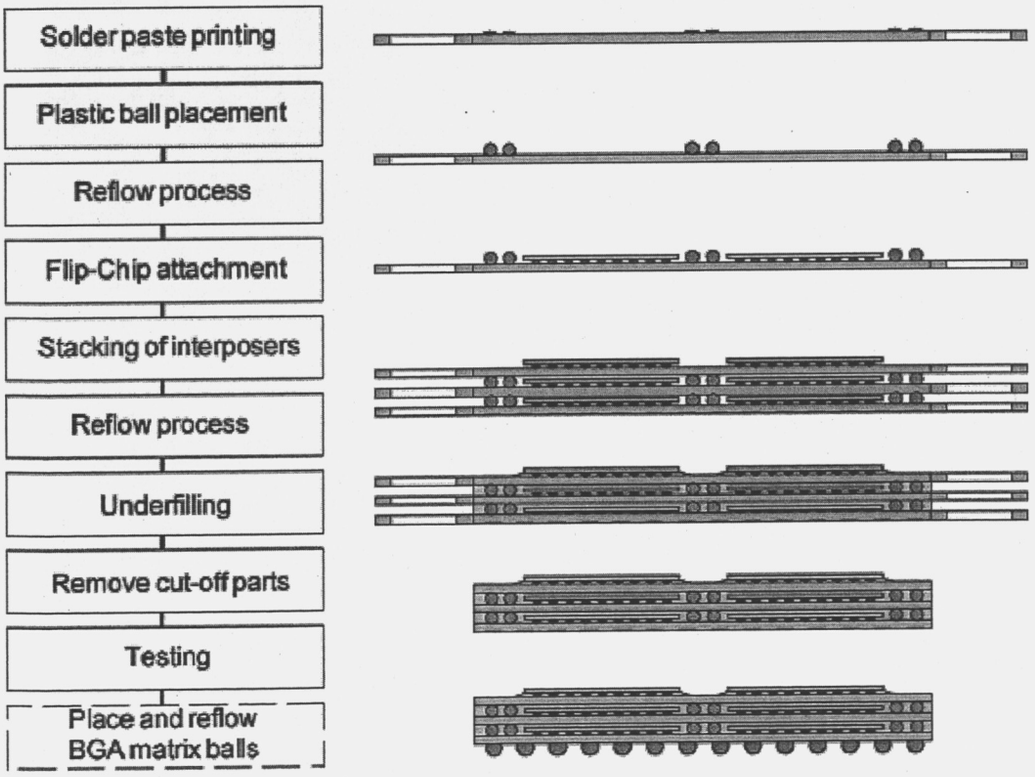



Figure 68. Process Sequence for MCMs Electrically Interconnected with Sn/Ag Plated Plastic Balls. [Pienimaa.pdf]

Fuzz buttons have also been used to interconnect stacked MCMs. The structure is illustrated in Figure 69 [Boudreaux.pdf]. Figure 70 illustrates the stack-up sequence. The

MCM substrate was polycrystalline diamond with thin film copper and polyimide layers fabricated on both sides. The Fuzz Button Board was a plastic retainer with 7200 holes. The gold plated fuzz buttons (Brillo Pads) were inserted into these holes. Figure 71 is a photograph of the Fuzz Button Board. Fuzz buttons provide a separable connection between the MCMs, providing an option for repair. As illustrated in Figure 69. compression bolts are required to maintain electrical contact between MCMs through the fuzz buttons.

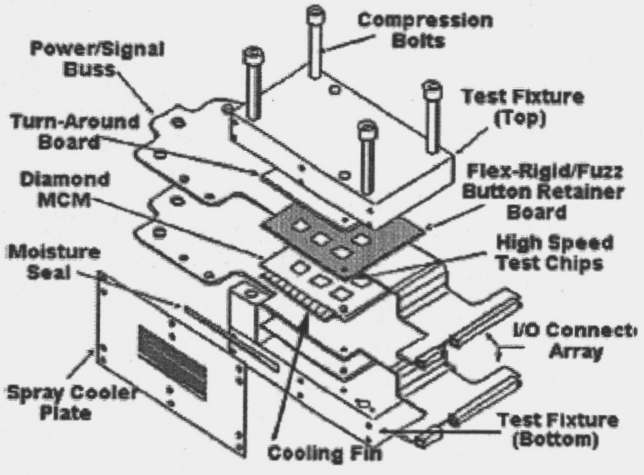



Figure 69. 3D MCM with Fuzz Button Layer-to-Layer Interconnections. [Boudreaux.pdf]

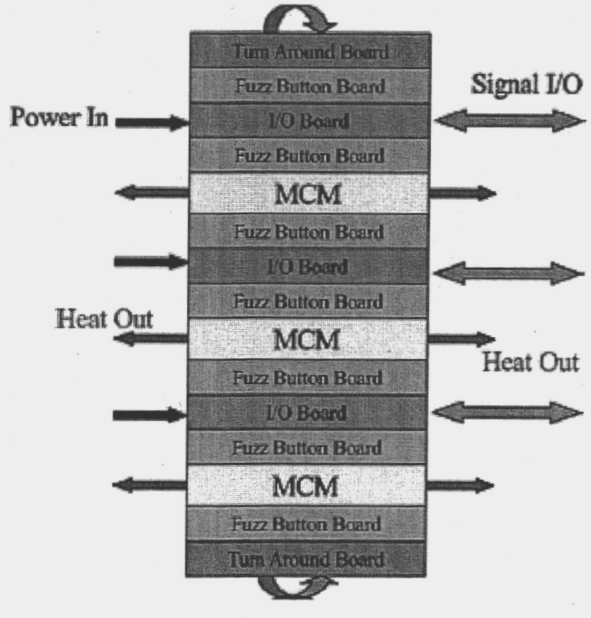



Figure 70. Illustration of MCM/Fuzz Button Board Stack-up. [Boudreaux.pdf]

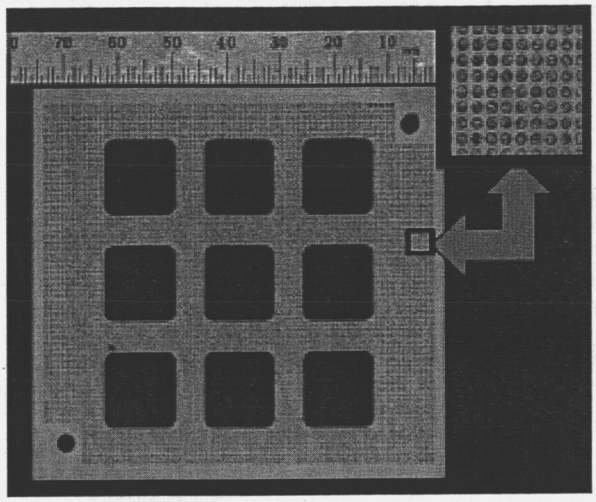


Figure 71. Photograph of the Fuzz Button Board. [Boudreaux.pdf]

Thales Microwave has developed a 3D T/R module [Favier.doc]. The construction is illustrated in Figure 72 [Favier]. The individual MCM layers are MCM-D with embedded $Ta_2O_5$ capacitors. Electrical connections between MCM layers are made with fuzz buttons.

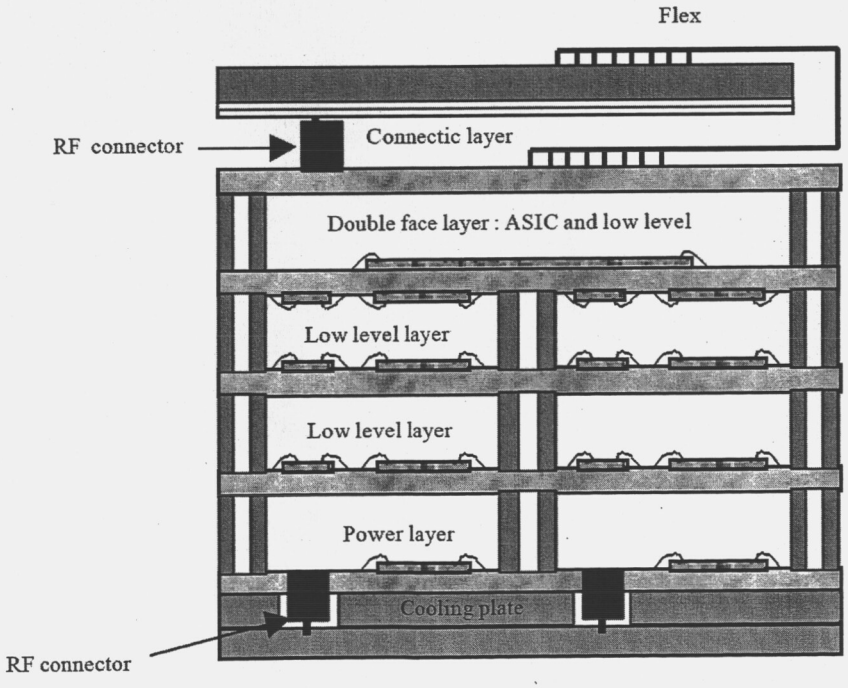



Figure 72. Illustration of Thales Microwave 3D MCM-D T/R Module. [Favier.doc]

The limitation of the edge routed 3D cubes is the number of interconnections available between layers and the requirement that signals be routed to the edge of the cube before routing to other layers, which adds signal delay. IMEC in Belgium has developed a 3D chip stacking technology with the potential for extension to 3D MCMs with z-direction connections distributed over the area of the MCM. The basic concept is shown in Figure 73 [Pinel.pdf]. The technology requires ultra-thin (~10-15μm) silicon die. The process sequence is shown in Figure 74 [Cazaux.pdf]. Figure 75 shows a photograph of interconnections to a 15μm thick die, while Figure 76 shows a cross section of a single die layer MCM. Since this is a sequential built-up process, known good die and high process yields are required. Thermal modeling of the structure has been performed [Pinel.pdf]. The die are embedded in BCB which has a low thermal conductivity. Thermal vias and metal heat spreaders can be used to improve thermal performance. Leseduarte, et al., have evaluated the stress on the thin silicon die assembled into the structure [Leseduarte.pdf]. The model results indicate a wide range of design freedom.

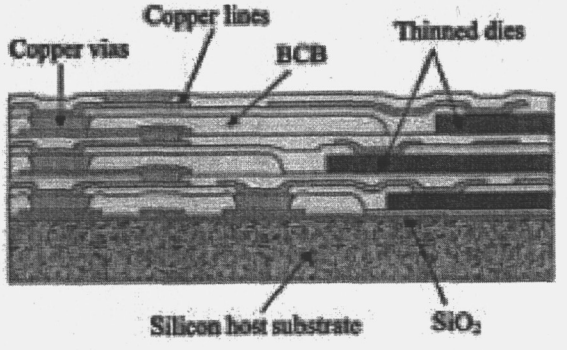



Figure 73. Illustration of IMEC 3D Packaging. [Pinel.pdf]

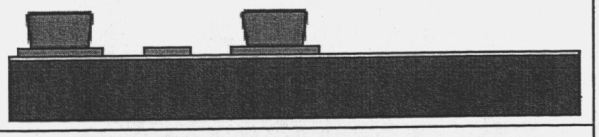
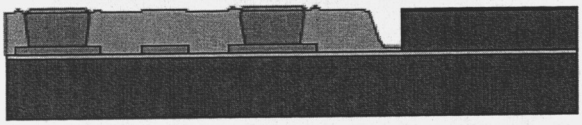
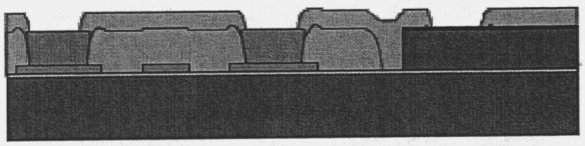
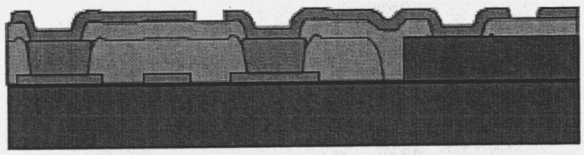
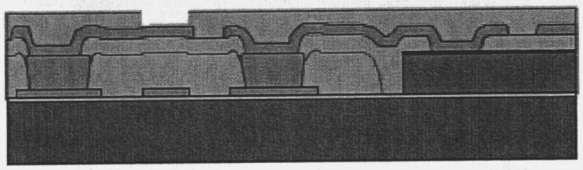
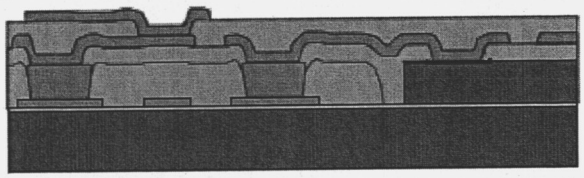
| | |
|---|---|
| Step 1 : Growth of copper studs. Patterning and wet etching of the first interconnection metallisation |  |
| Step 2 : Bonding of the ultra-thin die. Deposition of a thick photo-BCB layer : opening of vias on studs and "cavity" on the chip. |  |
| Step 3 : Deposition of second BCB layer. Dry etching to remove the BCB residues |  |
| Step 4 : Formation of the second metallisation layer |  |
| Step 5 : Deposition of an insulating and planarising BCB layer |  |
| Step 6 : Deposition of the contact metal layer for pad definition or proceed with step 1 for 2nd 'physical layer' |  |

Figure 74. Illustration of IMEC 3D Packaging Process Sequence. [Cazaux.pdf]

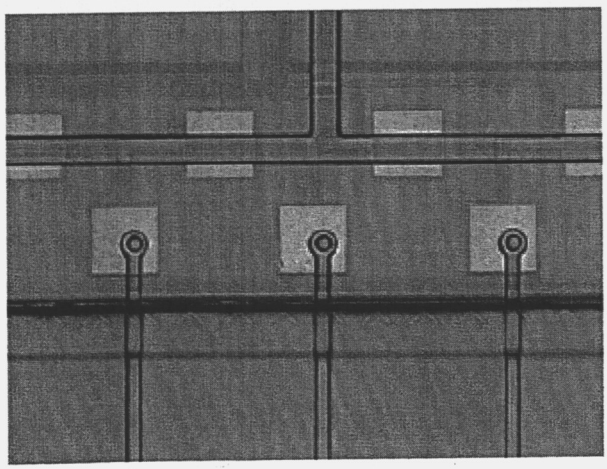


Figure 75. Photograph of thin Film Interconnect to a 15μm Thick Silicon Die. [Cazaux.pdf]

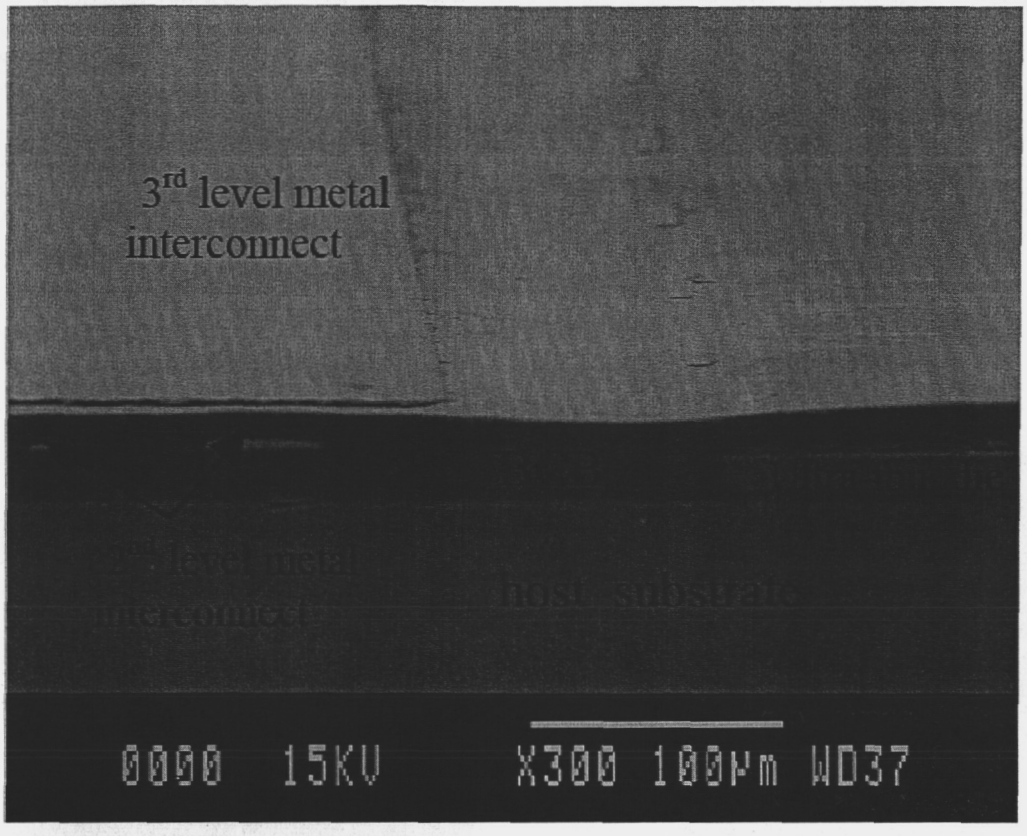



Figure 76. Cross Section of IMEC MCM with Single Die Layer. [Cazaux.pdf].

Working in collaboration, Auburn University, the Jet Propulsion Laboratory and Johns Hopkins University-Applied Physics Laboratory have demonstrated thinned silicon die assembled by flip chip on flexible substrates [Zhang.pdf]. Examples are shown in Figures 77 and 78. Both polyimide and liquid crystal polymer (LCP) flexible substrates have been used. Work is currently underway to demonstrate the 3D structure illustrated in Figure 79. Pre-tested assembled flex layers will be laminated and electrically interconnected to produce the 3D MCM.

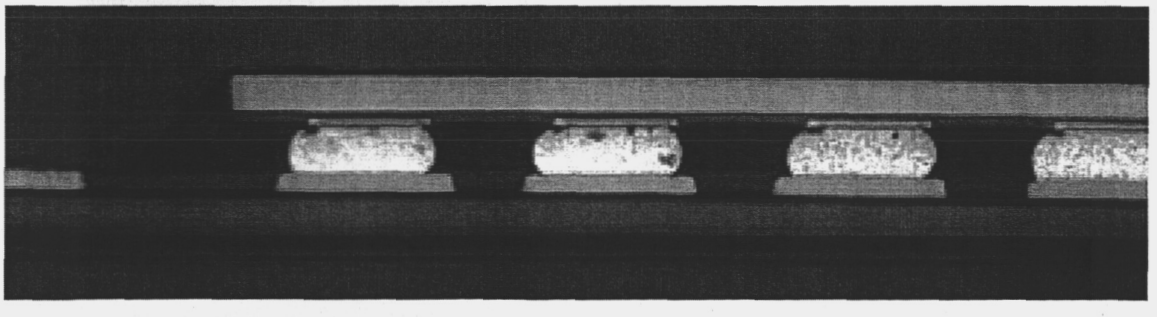


Figure 77. Cross Section of a 50µm Thick Silicon Die on 50µm Thick Polyimide Flex Substrate. [Zhang.pdf]

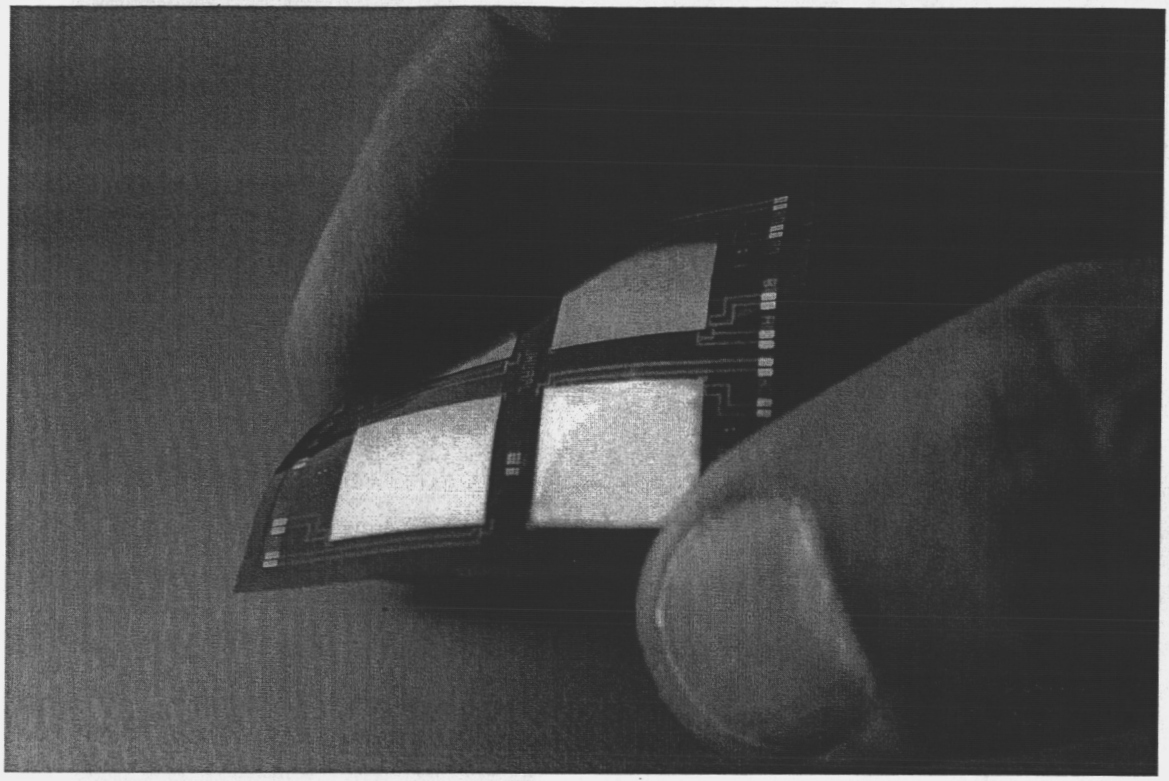
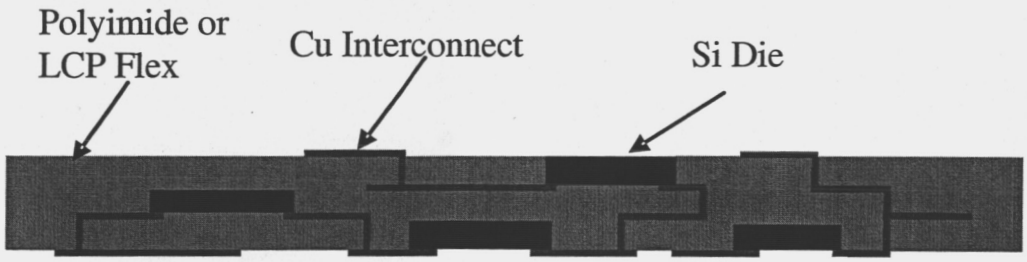


Figure 78. Photograph of 1cm x 1cm x 50μm Thick Silicon Die on 50μm Thick Polyimide Flex Substrate. [Zhang.pdf]




Figrue 79. Proposed 3D Multilayer Flex-based MCM Technology.

A similar approach using thinned die is being developed by Samsung and Yonsei University [Shin.pdf]. The concept is illustrated in Figure 80. Rather than using flip chip bonding, the die are thermocompression bonded to the flexible substrate. Electroplating is used to form the electrical interconnect.

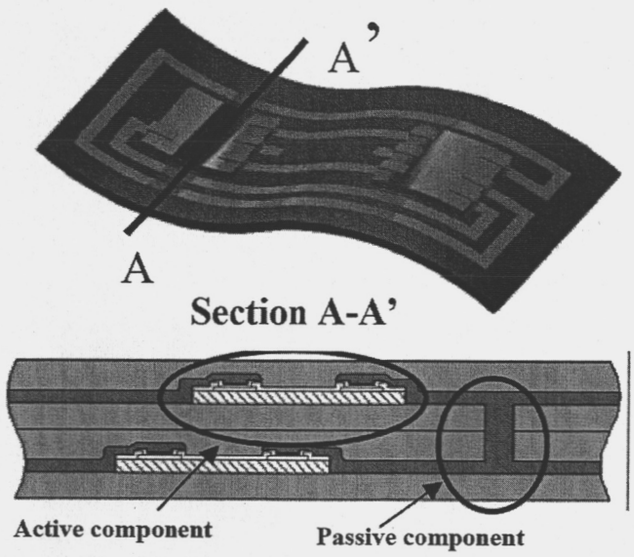



Figure 80. Illustration of Samsung/Yonsei university 3D Packaging Technology. [Shin.pdf]

Benefits of 3D MCMs: 3D MCMs provide a significant increase in functional density, decreasing size and weight. Interconnection lengths between devices are reduced, increasing signal speed. MCMs allow mixing and matching of different component technologies (digital, analog, rf, optical, Si, GaAs, passives, sensors, etc).

Limitations of 3D MCMs: Increasing functional density results in increasing power density, thus thermal management is an issue. Diamond substrates and integrated heat pipes are potential solutions to address heat removal, but additional work is required in this area for higher power 3D MCMs.

3D MCMs can potentially integrate a large number of die. As with other 3D technologies, die yield and know good die are a critical issue for 3D MCMs. Repair is possible in some 3D MCM technologies during the assembly process, but not after final assembly. Thus, system partitioning and good fault cover testing at the sub-assembly level is also important.

3D MCMs are custom products, thus the supplier base is much smaller than for stacked die or stacked packages. Furthermore, the 3D MCM technology used is specific to the supplier, resulting in effectively a single source situation.

Reliability of 3D MCMs: Reliability data is specific to the individual 3D MCM technologies. Although not completed at the time the paper was written, the Honeywell double sided MCM-C was to be screened for Space applications [Jensen.pdf]. The 3D-Plus MCM technology has been qualified by the European Space Agency [Val-1.pdf]. The approval test plan is shown in Figure 81. The 3D MCMs passed the tests outlined in the plan. The VIGOR 3D test vehicle pasted 500 thermal cycles (-55°C to +125°C) with the selection of the proper substrate and molding compounds [Alexandre.pdf]. Some material combinations tested in the experiment did not survive 500 cycles. The General

Electric 3D MCM technology was also developed targeting military and space reliability requirements [Saia.pdf]. The GE 3D MCMs have passed 100 cycles from liquid nitrogen (-193°C) to +125°C, 300 cycles from -65°C to +150°C and 22 hours of water soak at 85°C [Saia.pdf].

| Test | Method | Conditions |
|---|---|---|
| Electrical Test<br>Tmin, Tamb, Tmax | According to detal specifications for each TVs<br>*TV1; 3DPA0450-2 (Functional, DC & AC parameters)<br>*TV2: 3DPA0470-2 (Functional, DC et AC parameters)<br>* TV3: 3DPA0760-1(Functional, DC parameters) | |
| Workmanship Test<br>•Radiography<br>•Ext. visual inspection<br>•Dimensions measur. | <br>2012<br>2009 | According to Design files for each TVs |
| Temperature & Humidity under Bias (THB) | *1000hrs +85°C & 85°C under bias<br>•Electrical test at T0 (Tmin, Tamb, Tmax) , T0+240hrs & T0+500hrs (Tamb.), T0+1000hrs (Tmin, Tamb, Tmax)<br>* Drift calculation at Tamb | |
| Life test | 1005 | * Life test Bias and patterns According to Detail spec. for each TVs<br>* Electrical test at T0 (Tmin, Tamb, Tmax) , T0+168hrs, T0+500hrs & T0+1000hrs (Tamb.), T0+2000hrs (Tmin, Tamb, Tmax)<br>* Drift calculation at Tamb |
| Thermal cycles | -55°C/+125°C<br>Dwell time = 15mn<br>ramp=10°C/mn | * TV1 & TV2: 50 cycles<br>* TV3: 500 cycles<br>* Electrical test at Tamb after thermal cycles |
| Moisture resistance | 1004 | * Lead integrity is the initial condition of this test |
| Lead integrity | 2004 | Condition B1 |
| Solderability | 2003-7 | |
| Marking permanency | 2015-11 | Condition 2-1a |
| Final DPA | | According to 3D PLUS Procedure 3DPF2290 |
| Visual Inspection | | According to 3D PLUS Procedure 3300-0776 |

Figure 81. 3D-Plus Approval Plan. [Val-1.pdf]

Technology Readiness Level Assessment: The TRL is dependent on the specific 3D MCM technology. The 3D-Plus technology has been approved by the European Space Agency for "3D Stacking Technologies Modules for use in ESA space programmes" [Approval_ESA.pdf]. 3-D Plus modules have flown in satellites and rovers. This would indicate a high TRL number. Other technologies such as those being developed by IMEC, Auburn University and Samsung are in the developmental stages and are at a TRL of 2-3.

## Wafer Stacking

DARPA has funded the Vertically Integrated Sensor Arrays (VISA) program to develop stacked wafer technology. The applications driver for this technology is to develop real-time large area sensor arrays. The information in each pixel must be serially transferred to the edge of the array for processing. This limits the speed of large arrays. In the VISA program, wafers are to be stacked behind the sensor array so that pixel information can be transferred downward for processing in a massively parallel fashion. As shown in Figure 82, multiple sensors layers can also be included for visible and IR detection [Seshadri.pdf]. The resulting imaging system would be similar to human vision.

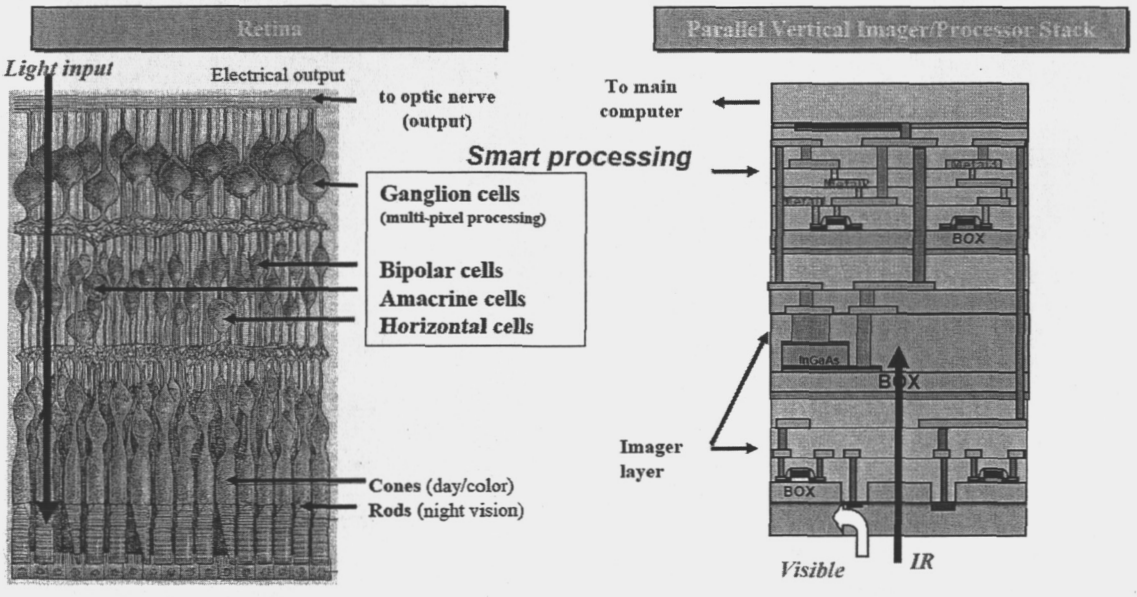



Figure 82. Comparison of 3-D Imaging with Human Sight. [Seshadri.pdf]

The MIT Lincoln Laboratories 3D technology is illustrated in Figures 83 – 86 [Keast.pdf]. The top wafers (wafers 2 and 3) are silicon-on-insulator (SOI) and in the process the underlying silicon is removed, leaving isolated devices surrounded by oxide. In the original process, adhesive (epoxy) was used to bond the wafers. This limited processing temperatures to <200°C. A low temperature oxide bond is now used by MIT Lincoln Laboratories, allowing higher temperature processing in subsequent steps. Low pressure chemical vapor deposited (LPCVD) oxide layers deposited on each wafer are used as the bond layers. The two LPCVD oxide layers are bonded together at 275°C for 10 hours. Chemical vapor deposited (CVD) tungsten plugs are used for the wafer-to-wafer interconnection. In the last step, bond pads are opened to allow packaging of the 3D device by conventional wire bonding.

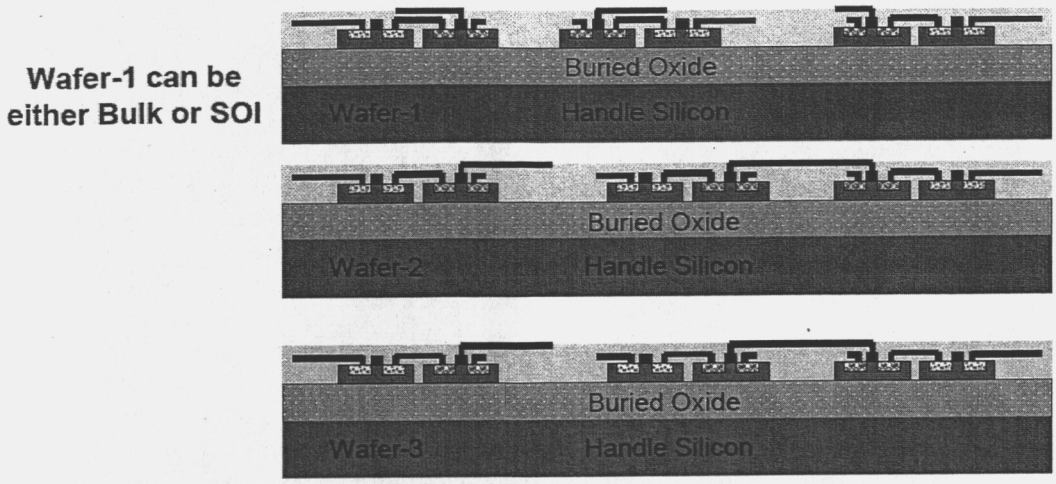
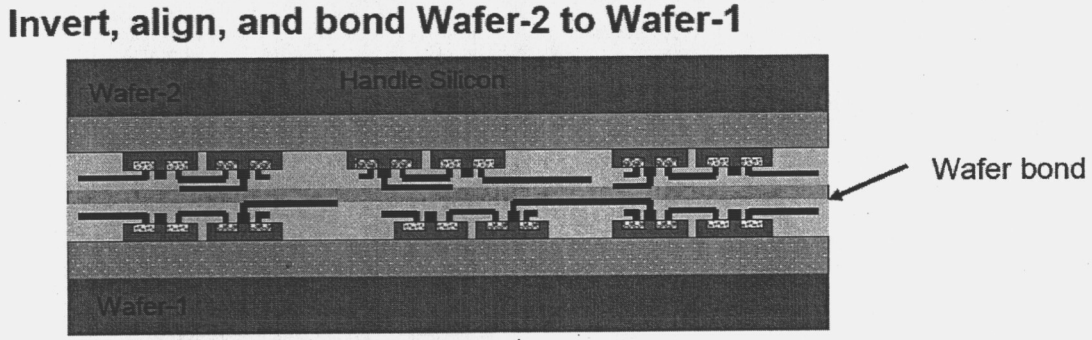



Figure 83. Starting Wafers in MIT Lincoln Laboratories 3D Process. [Keast.pdf]



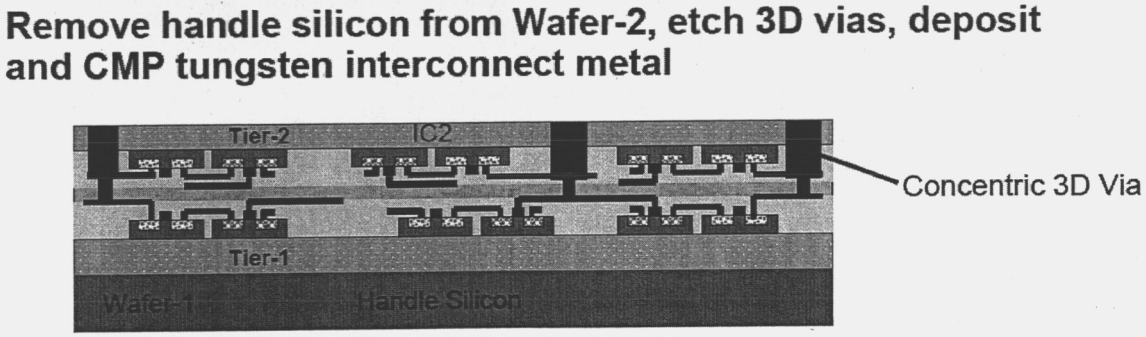
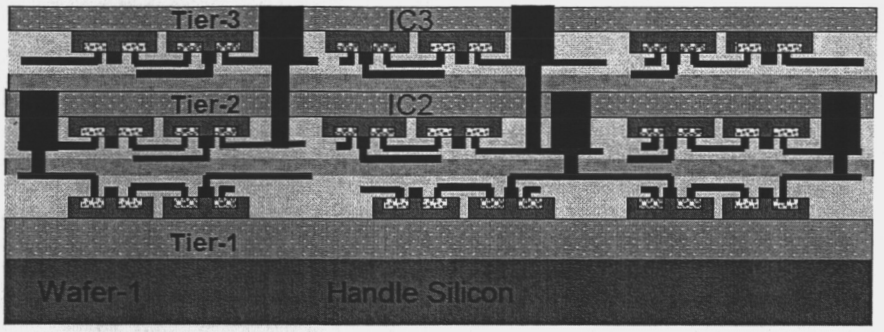




Figure 84. Wafer 1 to Wafer 2 Alignment, Bonding and Interconnection. [Keast.pdf]

## Invert, align, and bond Wafer-3 to Wafer-2/1-assembly, remove Wafer-3 handle wafer




## Etch Bond Pads

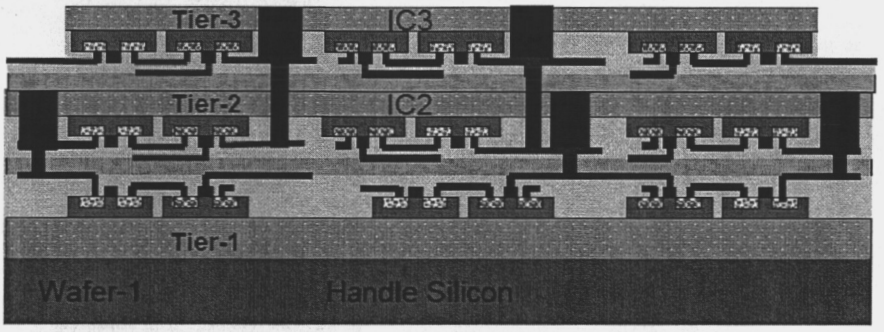



Figure 85. Wafer 3 Alignment, Bonding and Interconnection. [Keast.pdf]

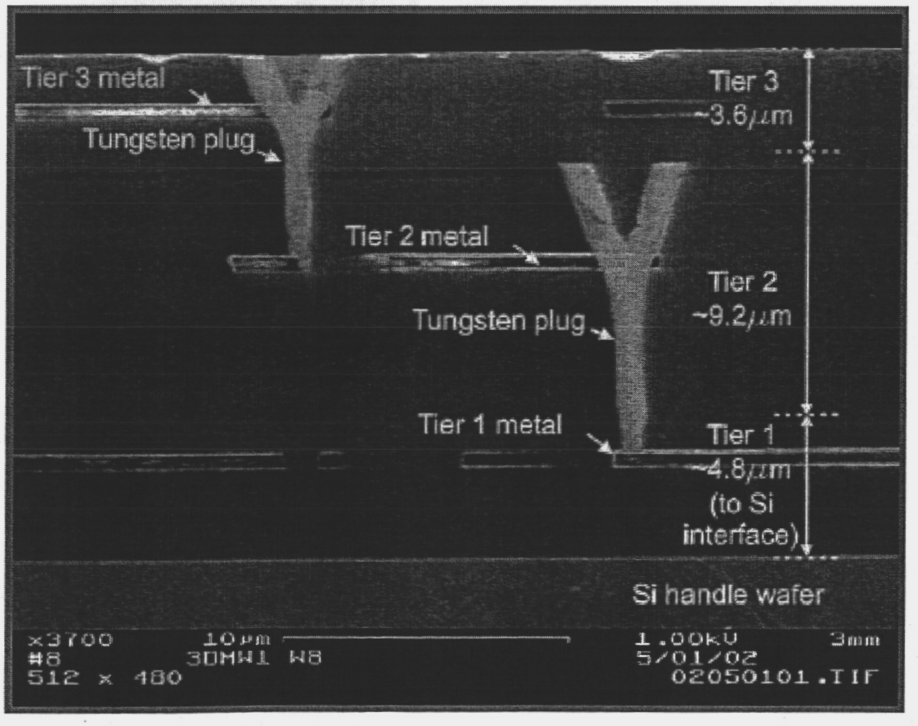



Figure 86. Cross-Section of Three Wafer Stack. [Keast.pdf]

A number of research groups are working to develop 3D wafer stacking technology including IBM [Guarini.pdf], Tezzaron Semiconductor [Patti.pdf], the University of Arkansas, Ziptronix [Markunas.pdf], and Raytheon Visions Systems/University at Albany [Fletcher]. The Raytheon/University of Albany approach uses benzocyclobutene as the adhesive layer between wafers. Tezzaron, the University of Arkansas and others are developing through wafer technology with plated copper interconnections. A cross section of the Tezzaron Cu interconnects is shown in Figure 87.

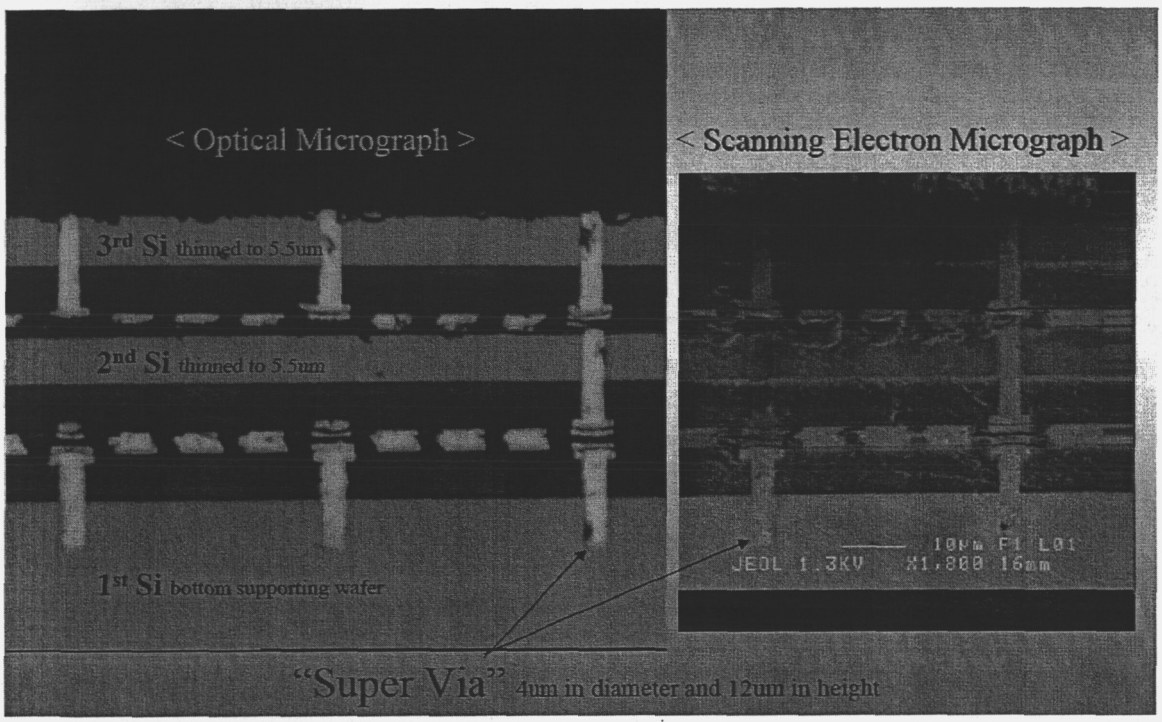



Figure 87. Cross Section of Tezzaron Cu Metallized Vias. [Patti.pdf]

Benefits of Wafer Stacking: Wafer stacking provides a true 3-D interconnect structure, allowing highly parallel signal processing. It is particularly suitable for image processing, and is being considered as a way to extend Moore's Law for high performance processors and memory. The electrical performance benefits of short, 3-D interconnections have also been modeled for a RIC Processor/Cache System [Kuhn.pdf].

Limitations of Wafer Stacking: Wafers must be designed for compatibility with wafer stacking. Thus, the approach is not suitable for low volume applications unless it is an extremely high value added application. As with other 3-D stacking technologies, thermal management will be a major challenge. In the MIT-Lincoln Laboratories structure, the SOI transistors are surrounded by silicon dioxide, which has a low thermal conductivity. Rahman has shown that the power dissipation in 3-D ICs is lower due to less parasitic interconnection capacitance [Rahman.pdf]. Thus, lower power operation is one advantage and potential thermal benefit of 3-D wafer stacking.

Yield will be a major challenge. Each wafer will have an individual yield and in many cases, a good die on one wafer will align with a defective die on another wafer in the stack. Wafer mapping and sorting may be used to optimize stacked yield. Ziptronix has developed a hybrid approach to achieve higher final yield. In this approach, pre-tested die are stacked onto a pre-tested base wafer (Figure 88). Ziptronix [Markunas.pdf] has patented a pre-treatment that allows room temperature, covalent oxide-to-oxide bonding of the die to the base wafer. Figure 89 shows an 'over the edge' interconnect of a 10μm thick die to the base substrate. A planarization step allows thin film processing of the interconnections. Ziptronixs has also developed thru-wafer interconnections as shown in Figure 90.

Klumpp, et al. have also developed a chip-on-wafer approach [Klumpp.pdf]. The process flow is shown in Figure 91. The process uses W metallized vias through thinned die to achieve back side electrical contact. Cu-Sn intermetallic bonding is used to bond the die to the wafer and to provide electrical interconnections.

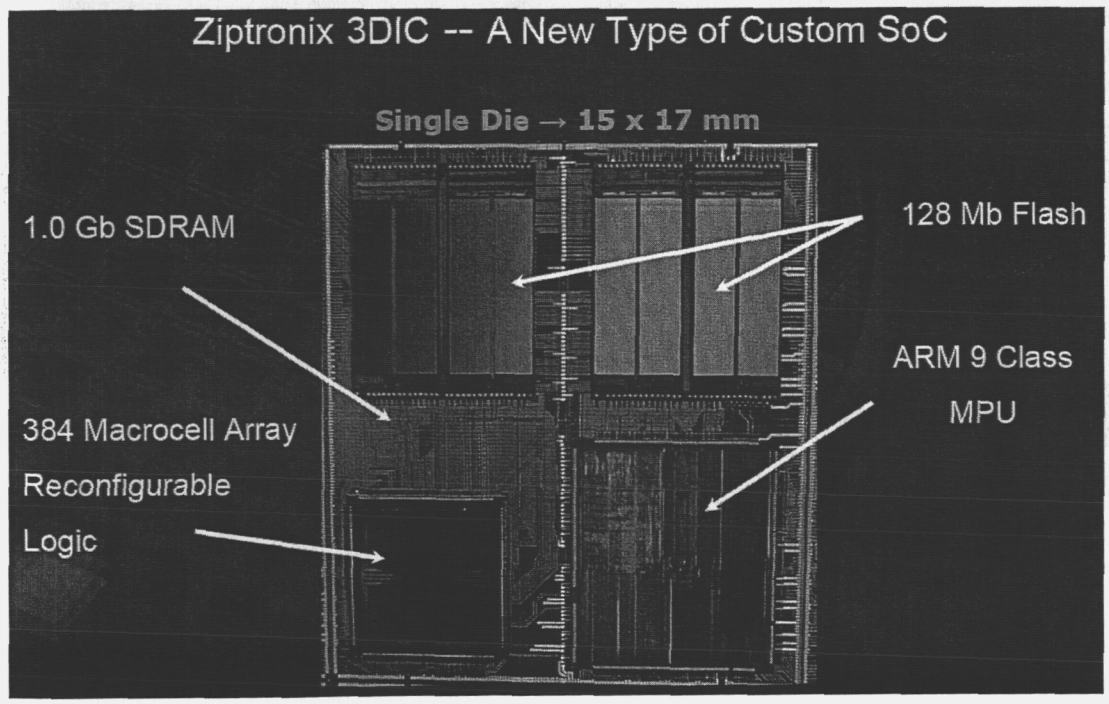



Figure 88. Photograph of Ziptronix Hybrid 3D Stacking Approach. [Markunas.pdf]

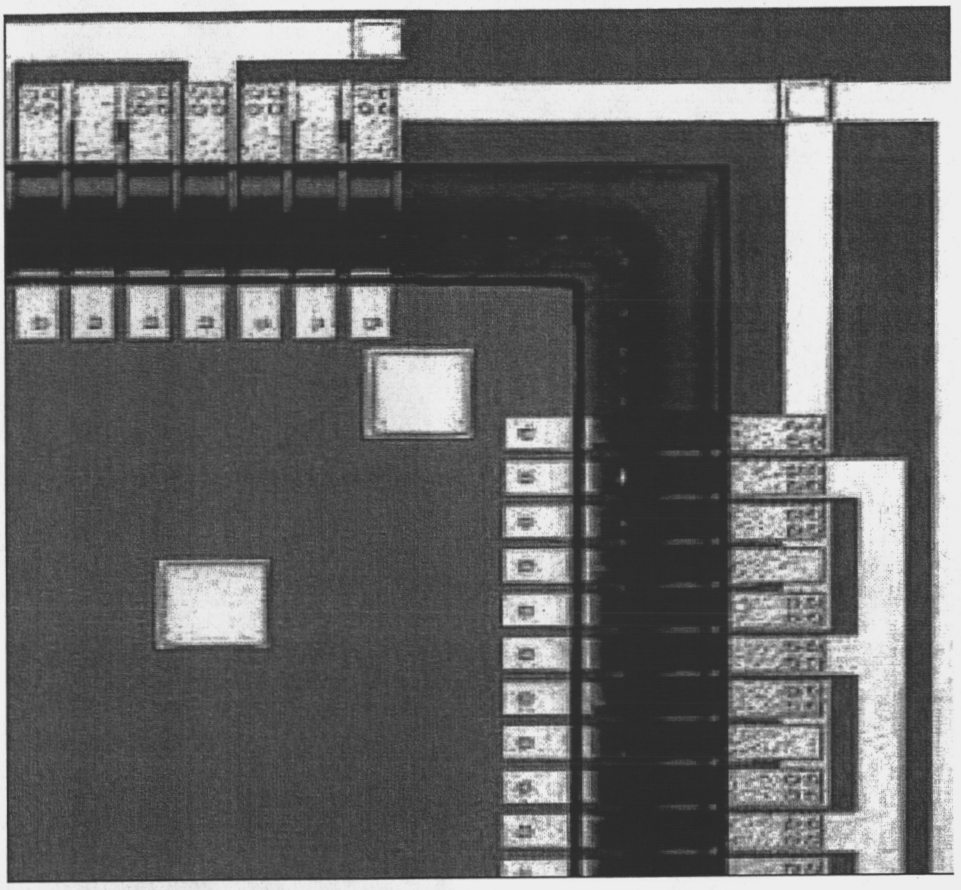


Figure 89. Example of Over the Edge Interconnection. [Markunas.pdf]

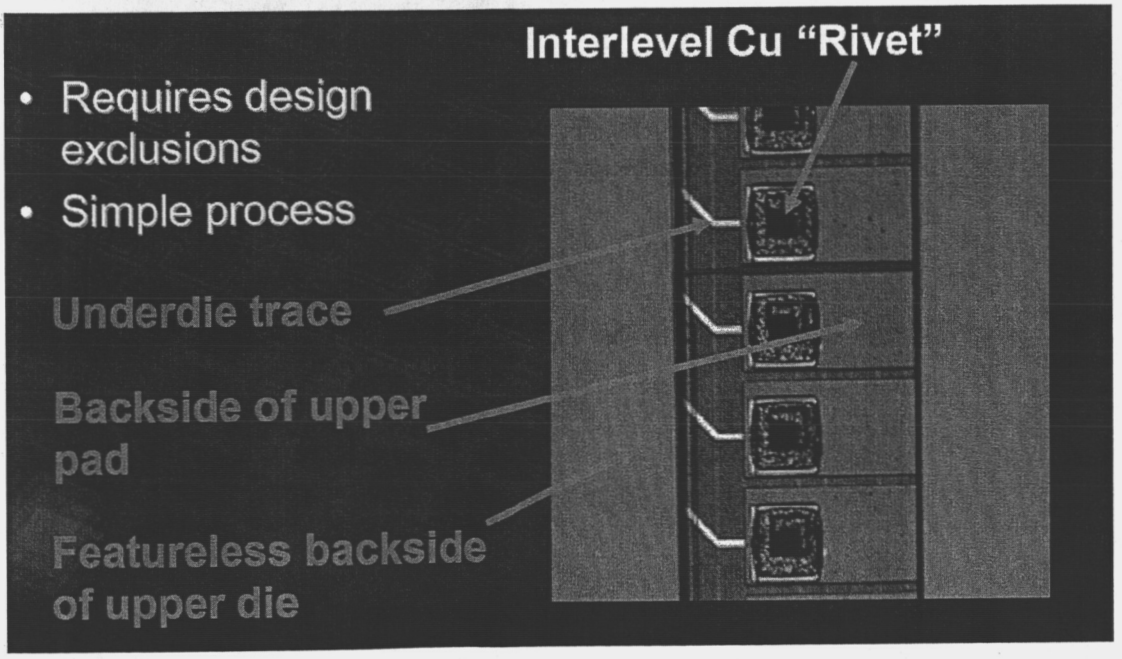



Figure 90. Example of Through Silicon Interconnections. [Markunas.pdf]

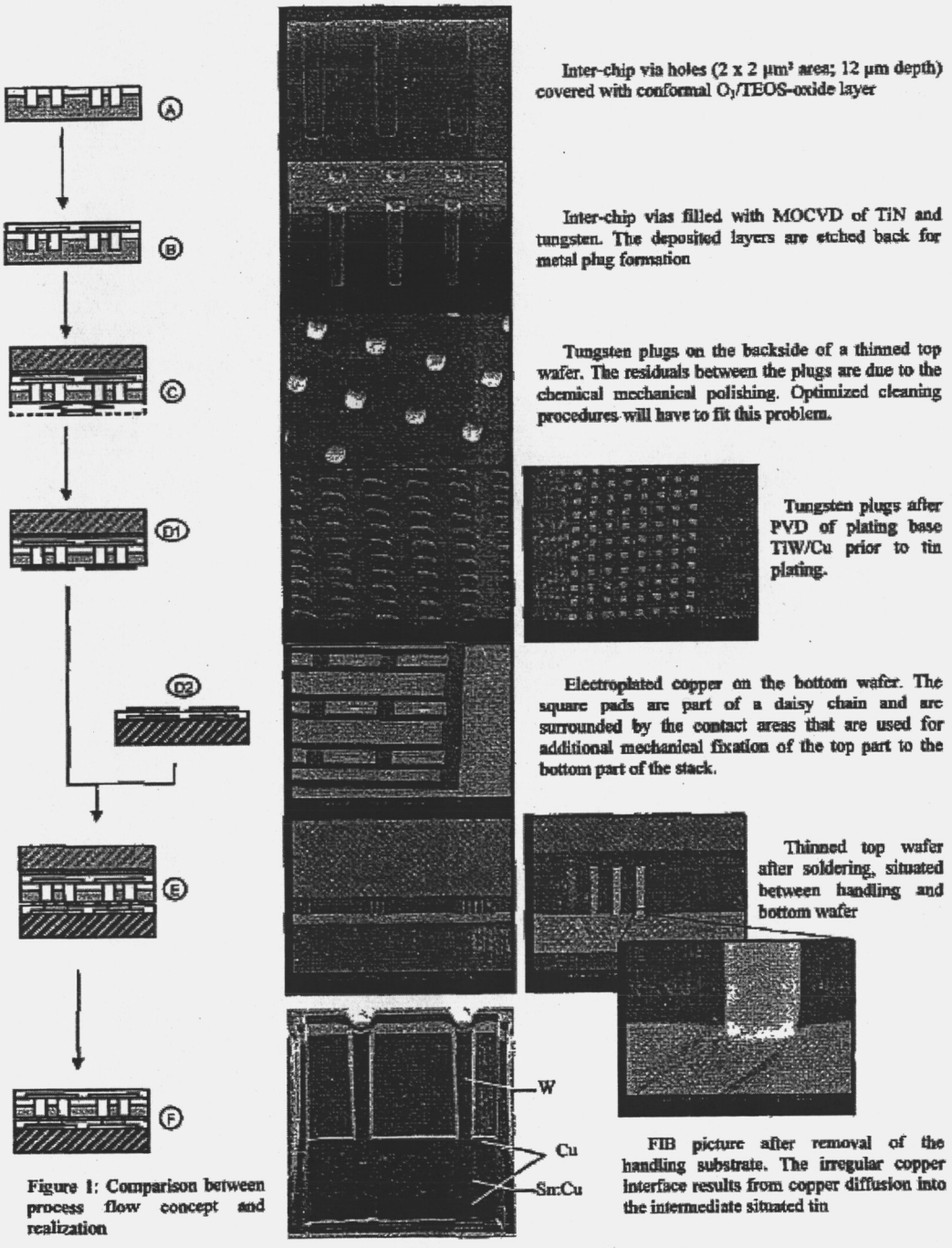



Figure 91. Chip-on-Wafer 3D Process Flow. [Klumpp.pdf]

Technology Readiness Level Assessment: Wafer stacking is in the development stage. Basic processes have been demonstrated, but are still being refined. Little reliability testing has been performed. Based on the current state of the art, the Technology Readiness Level Assessment is TRL-1.

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